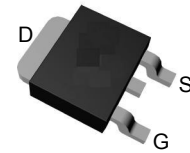


N-Channl Enhancement Mode MOSFET

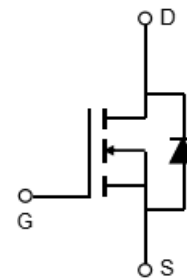
- 30V/100A
- $R_{DS(ON)}=3m\Omega$ (typ) @VGS=10V
 $R_{DS(ON)}=4.5m\Omega$ (typ) @VGS=4.5V
- 100% UIS & RG Tested
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Power Management for Industrial Converters

Pin Configuration

Top View of TO-252-2



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Rating	Unit
Common Ratings				
V _{DSS}	Drain-Source Voltage		30	V
V _{GSS}	Gate-Source Voltage		±20	
I _D	Continuous Drain Current	Tc=25°C	100	A
		Tc=100°C	39	
I _{DM}	Pulsed Drain Current	Tc=25°C	160	
P _D	Power Dissipation	T _A =25°C	3.6	W
P _D	Power Dissipation	T _C =25°C	52	W
T _{STG} , T _j	Storage Temperature Range		-55 to 150	°C
I _D	Continuous Drain Current	T _A =25°C	18	A
		T _A =70°C	14	

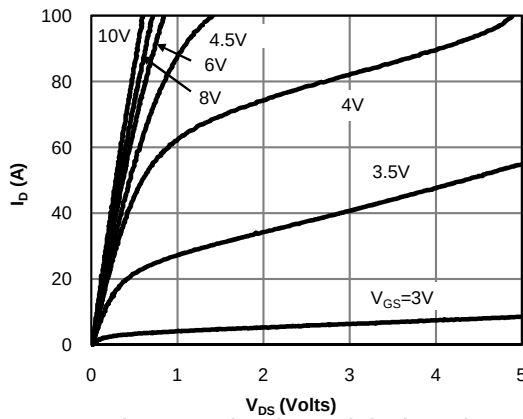
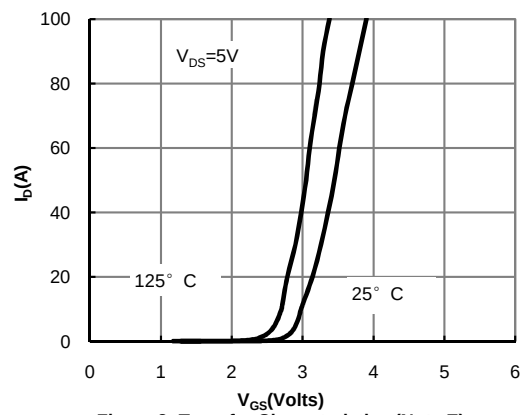
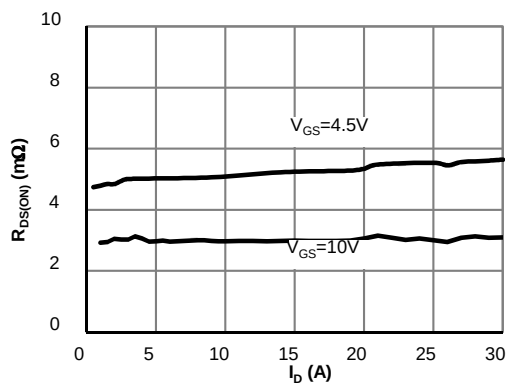
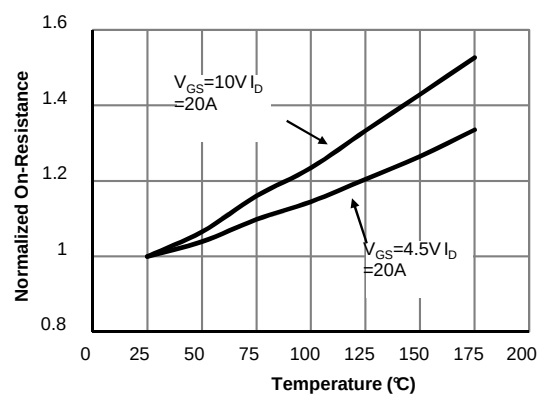
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V	-	-	1	μA
		T _j =85°C	-	-	30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1	-	2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)}	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	3	4.5	mΩ
		V _{GS} =4.5V, I _{DS} =15A	-	4.5	6.8	
Body Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} =40A, V _{GS} =0V	-	0.7	1.3	V
Dynamic Characteristics ^e						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =10V, Frequency=1.0MHz	-	3906	-	pF
C _{oss}	Output Capacitance		-	155	-	
C _{iss}	Reverse transfer capacitance		-	135	-	
t _{d(ON)}	Turn-on delay Time	V _{GS} =10V ,V _{DS} =15V R _G =1.8Ω, I _D =20A , R _L =30Ω	-	8	-	nS
t _r	Turn-on rise Time		-	9	-	
t _{d(OFF)}	Turn-off delay Time		-	32	-	
t _f	Turn-off rise Time		-	6	-	
Gate Charge Characteristics ^e						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _{DS} =20A	-	23	-	
Q _{gs}	Gate-Source Charge		-	5	-	
Q _{gd}	Gate-Drain Charge		-	3	-	

Note: 1. Pulse test: pulse width $\leq$ 300 μ S, duty cycle $\leq$ 2%

2.Static parameters are based on package level with recommended wire bonding

TYPICAL CHARACTERISTICS (25°C Unless Note)

Fig 1: On-Region Characteristics (Note E)

Figure 2: Transfer Characteristics (Note E)

Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

Figure 4: On-Resistance vs. Junction Temperature (Note E)

TYPICAL CHARACTERISTICS (continuous)

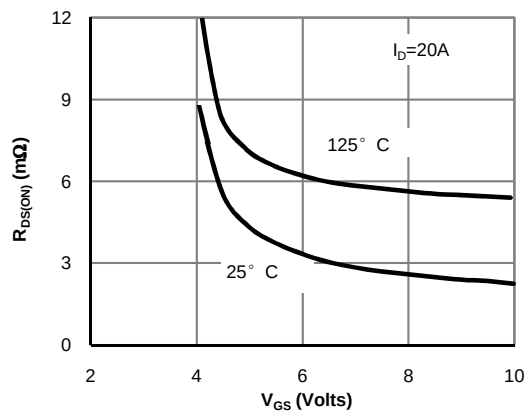


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

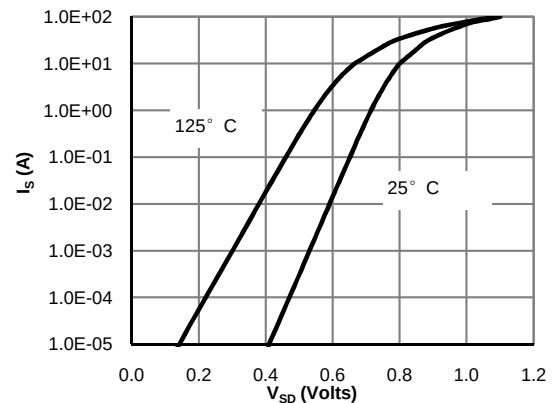


Figure 6: Body-Diode Characteristics (Note E)

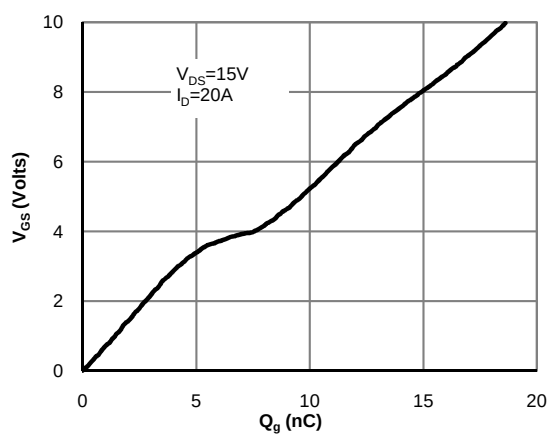


Figure 7: Gate-Charge Characteristics

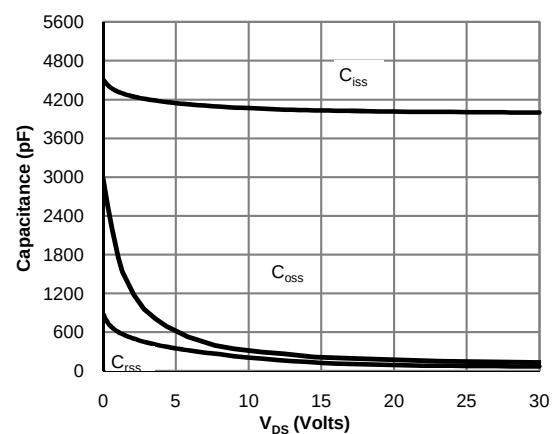


Figure 8: Capacitance Characteristics

TYPICAL CHARACTERISTICS (continuous)

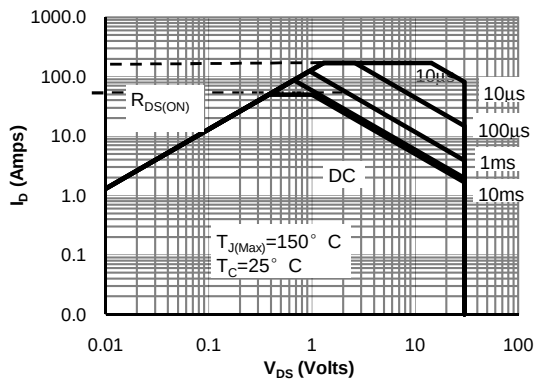


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

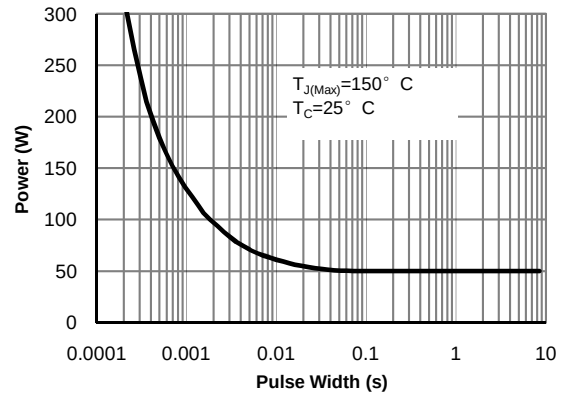


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

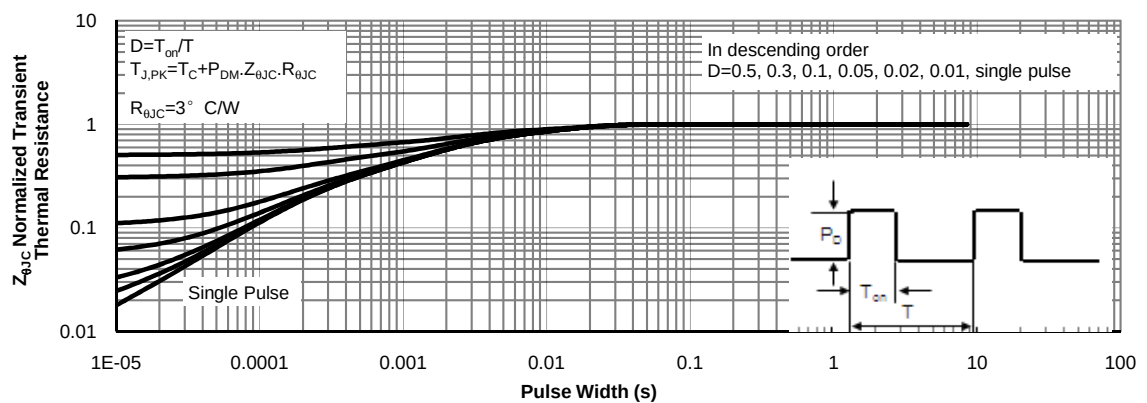
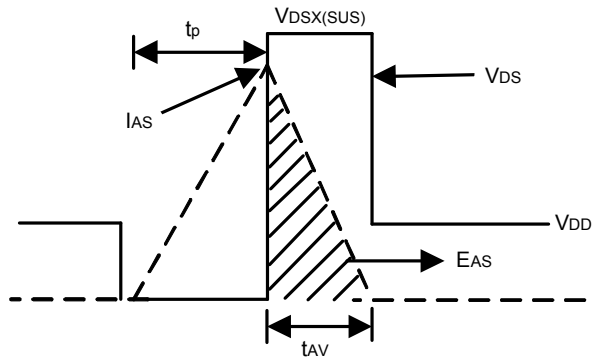
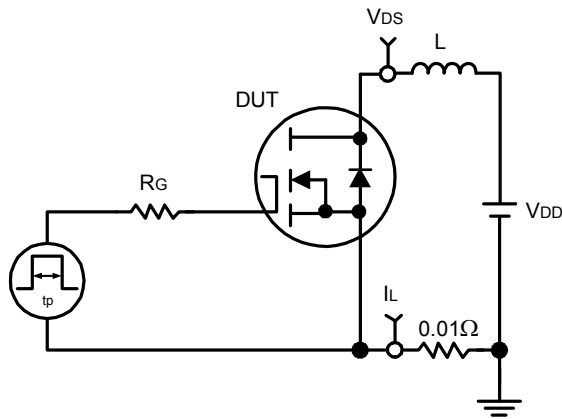
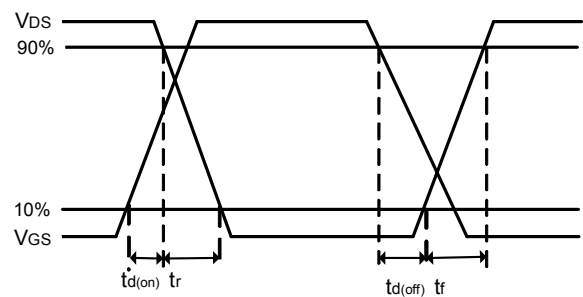
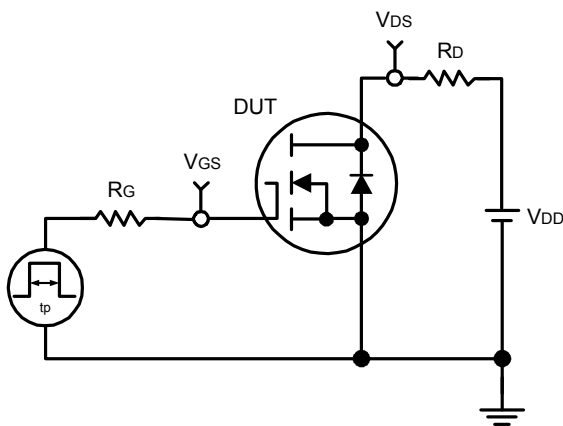


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Avalanche Test Circuit and Waveforms

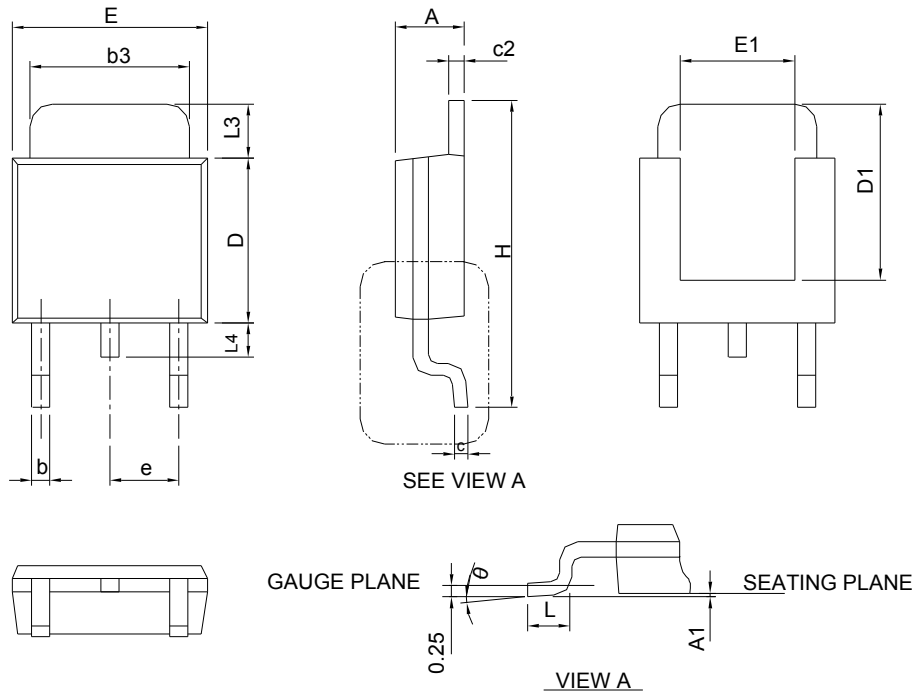


Switching Time Test Circuit and Waveforms



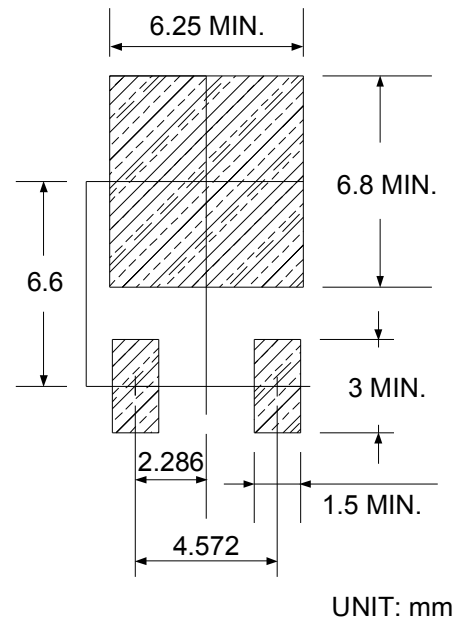
Package Information

TO-252-2



SYMBOL	TO-252-2			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	-	0.13	-	0.005
b	0.50	0.89	0.020	0.035
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	0.90	1.78	0.035	0.070
L3	0.89	2.03	0.035	0.080
L4	-	1.02	-	0.040
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note : Follow JEDEC TO-252-2 .