

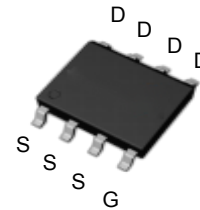
Features

- 100V/9A,
 $R_{DS(ON)} = 9 \text{ m}\Omega(\text{typ.}) @ V_{GS} = 10\text{V}$
 $R_{DS(ON)} = 11\text{m}\Omega(\text{typ.}) @ V_{GS} = 4.5\text{V}$
- 100% UIS + R_g Tested
- Reliable and Rugged
- Lead Free and Green Devices Available
 (RoHS Compliant)

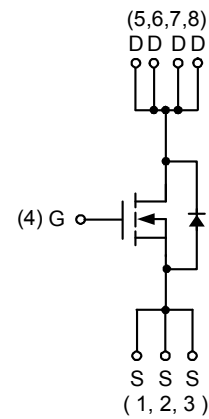
Applications

- Power Management for SMPS.
- DC-DC Converter.

Pin Description



Top View of SOP-8



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter		Rating	Unit
Common Ratings				
V _{DSS}	Drain-Source Voltage		100	V
V _{GSS}	Gate-Source Voltage		±20	
T _J	Maximum Junction Temperature		150	°C
T _{STG}	Storage Temperature Range		-55 to 150	
I _S ^c	Diode Continuous Forward Current	T _A =25°C	9	A
I _D ^c	Continuous Drain Current	T _A =25°C	9	A
		T _A =70°C	6.75	
I _{DM} ^a	Pulsed Drain Current	T _A =25°C	27	
P _D ^c	Maximum Power Dissipation	T _A =25°C	3.1	W
		T _A =70°C	2.0	
R _{θJA} ^c	Thermal Resistance-Junction to Ambient	t ≤ 10s	40	°C/W
		Steady State	80	°C/W
I _{AS} ^b	Avalanche Current, Single pulse	L=0.5mH	25	A
E _{AS} ^b	Avalanche Energy, Single pulse	L=0.5mH	156	mJ

Note a : Pulse width limited by maximum junction temperature.

Note b : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_J=25^\circ\text{C}$).

Note c : Surface Mounted on 1in^2 pad area, $t \leq 10\text{s}$

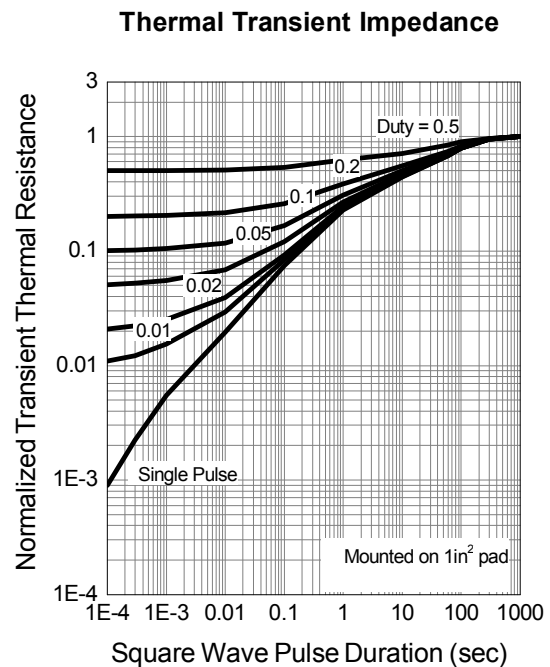
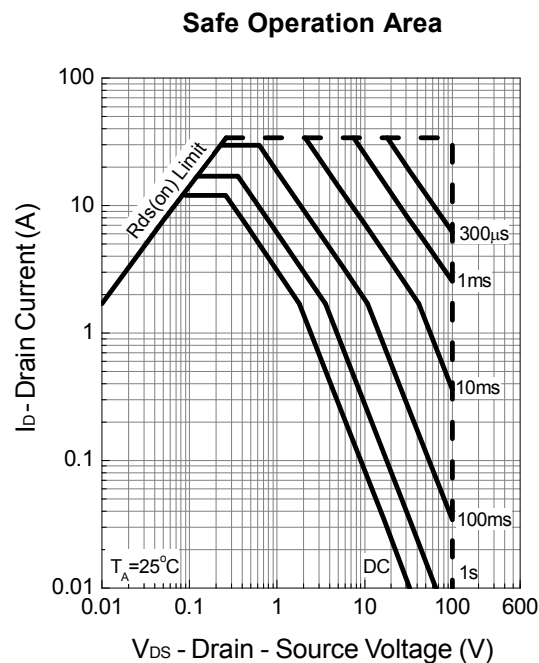
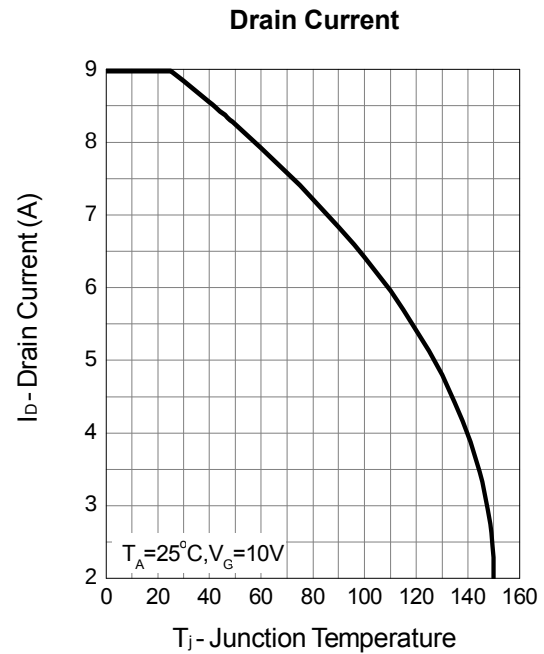
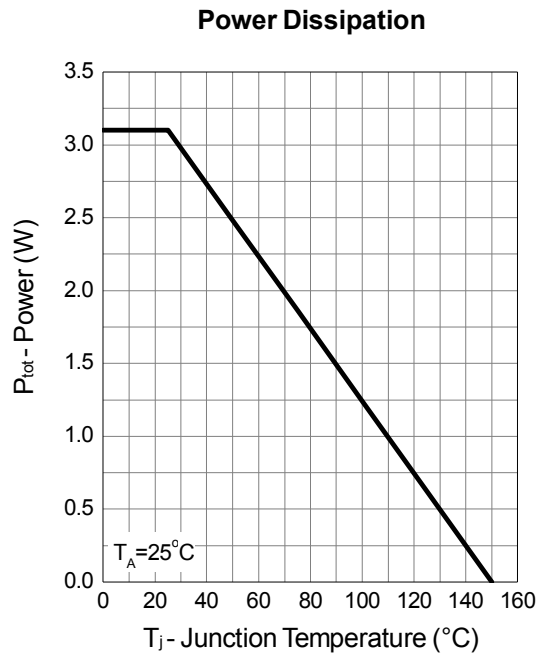
Electrical Characteristics (T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	100	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =80V, V _{GS} =0V T _J =85°C	-	-	1 30	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1	2	3	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^d	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =9A V _{GS} =4.5V, I _{DS} =6A	- -	9 11	12 14	mΩ mΩ
Diode Characteristics						
V _{SD} ^d	Diode Forward Voltage	I _{SD} =2A, V _{GS} =0V	-	0.8	1.3	V
t _{rr}	Reverse Recovery Time	I _{SD} =9A, dI _{SD} /dt=100A/μs	-	52	-	ns
Q _{rr}	Reverse Recovery Charge		-	82	-	nC
Dynamic Characteristics ^e						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	-	1.0	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, Frequency=1.0MHz	-	1964	2310	pF
C _{oss}	Output Capacitance		-	587	-	
C _{rss}	Reverse Transfer Capacitance		-	43	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =30V, R _L =30Ω, I _{DS} =1A, V _{GEN} =10V, R _G =6Ω	-	15	27	ns
t _r	Turn-on Rise Time		-	9	17	
t _{d(OFF)}	Turn-off Delay Time		-	51	92	
t _f	Turn-off Fall Time		-	65	117	
Gate Charge Characteristics ^e						
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =4.5V, I _{DS} =9A	-	22	-	nC
Q _g	Total Gate Charge	V _{DS} =50V, V _{GS} =10V, I _{DS} =9A	-	44	62	
Q _{gs}	Gate-Source Charge		-	8	-	
Q _{gd}	Gate-Drain Charge		-	9	-	

Note d : Pulse test ; pulse width≤300μs, duty cycle≤2%.

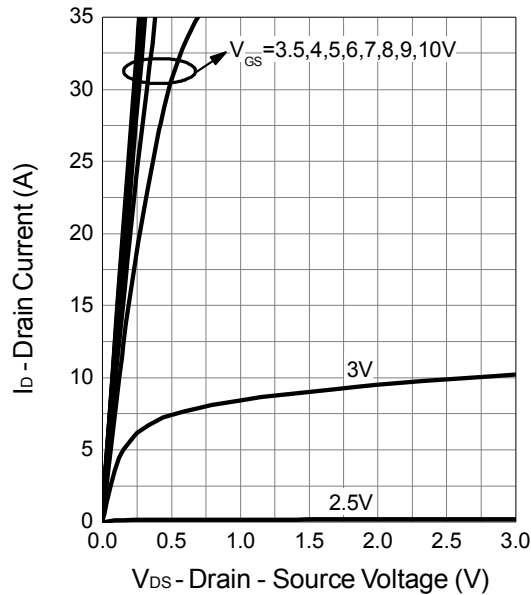
Note e : Guaranteed by design, not subject to production testing.

Typical Operating Characteristics

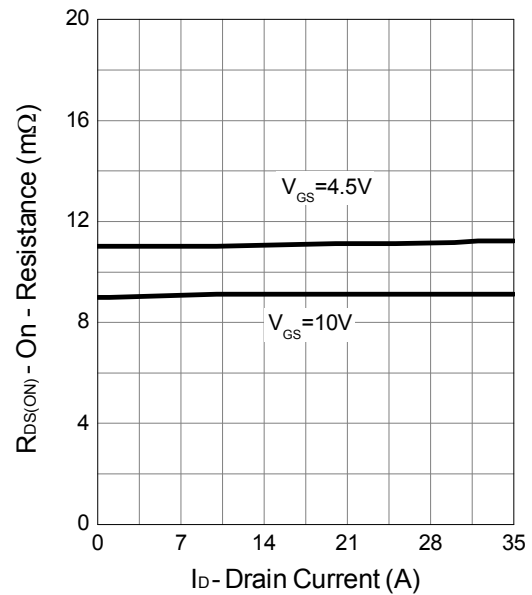


Typical Operating Characteristics (Cont.)

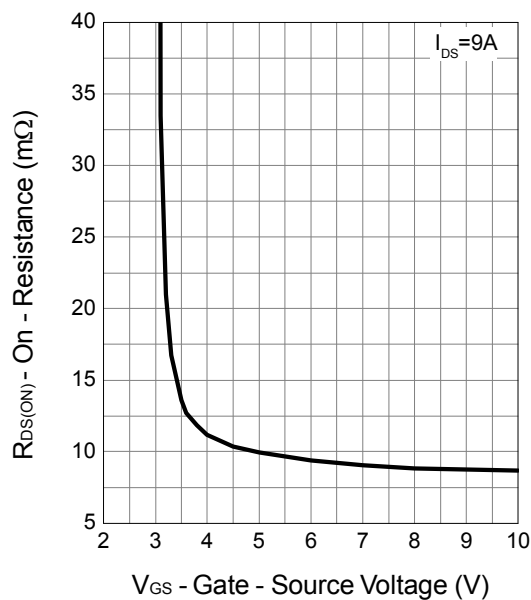
Output Characteristics



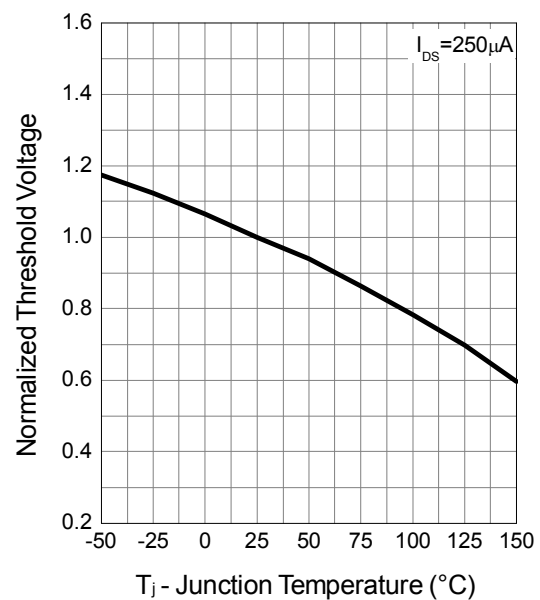
Drain-Source On Resistance



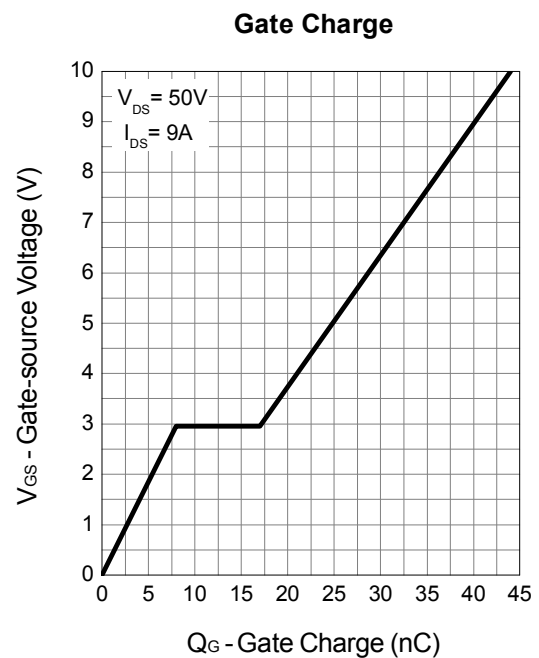
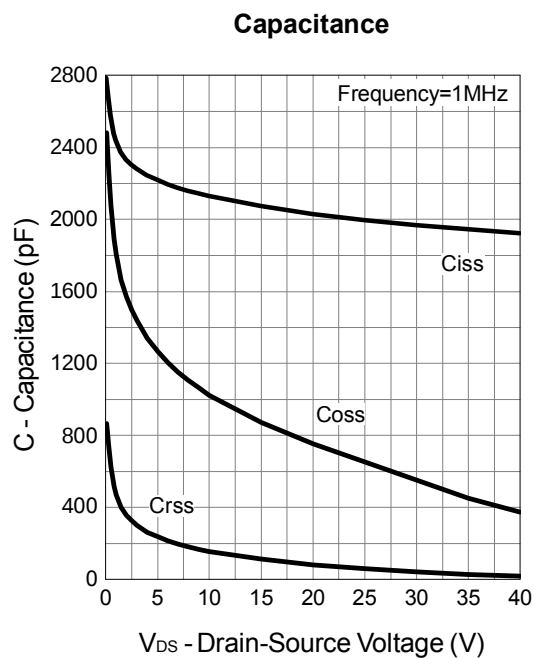
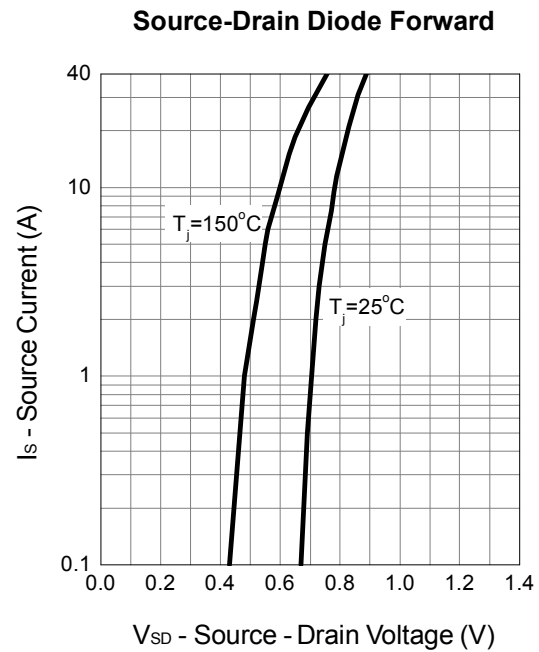
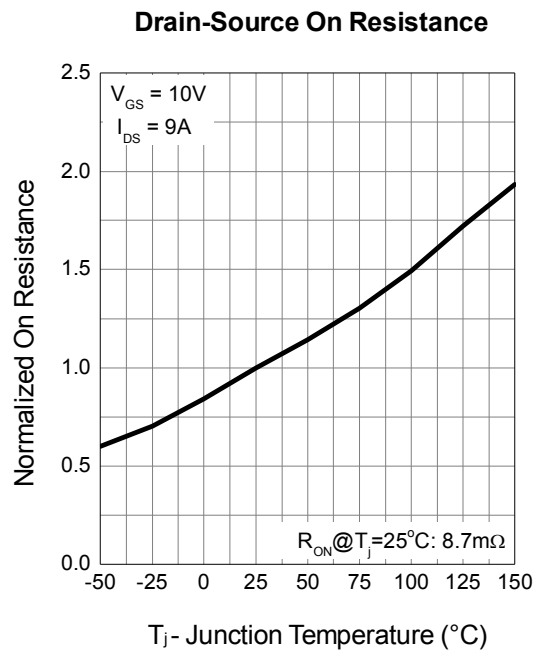
Gate-Source On Resistance



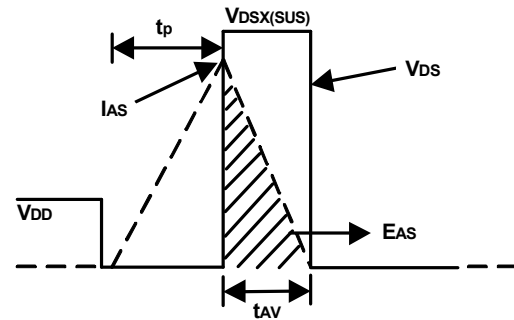
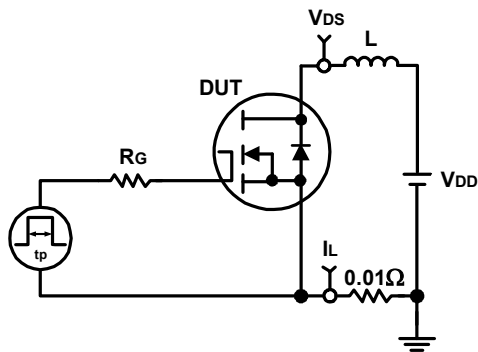
Gate Threshold Voltage



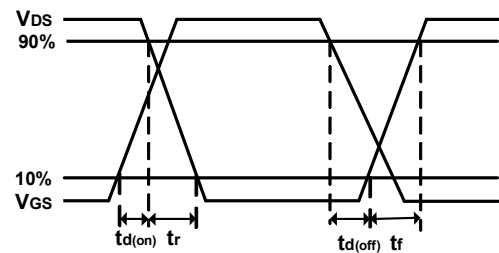
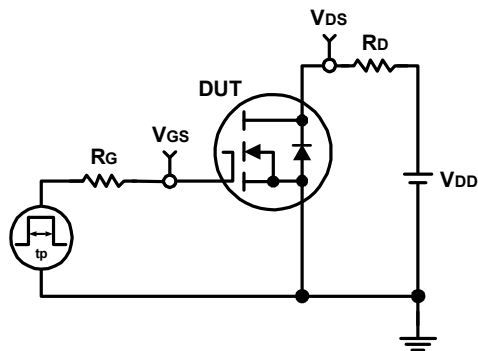
Typical Operating Characteristics (Cont.)



Avalanche Test Circuit and Waveforms

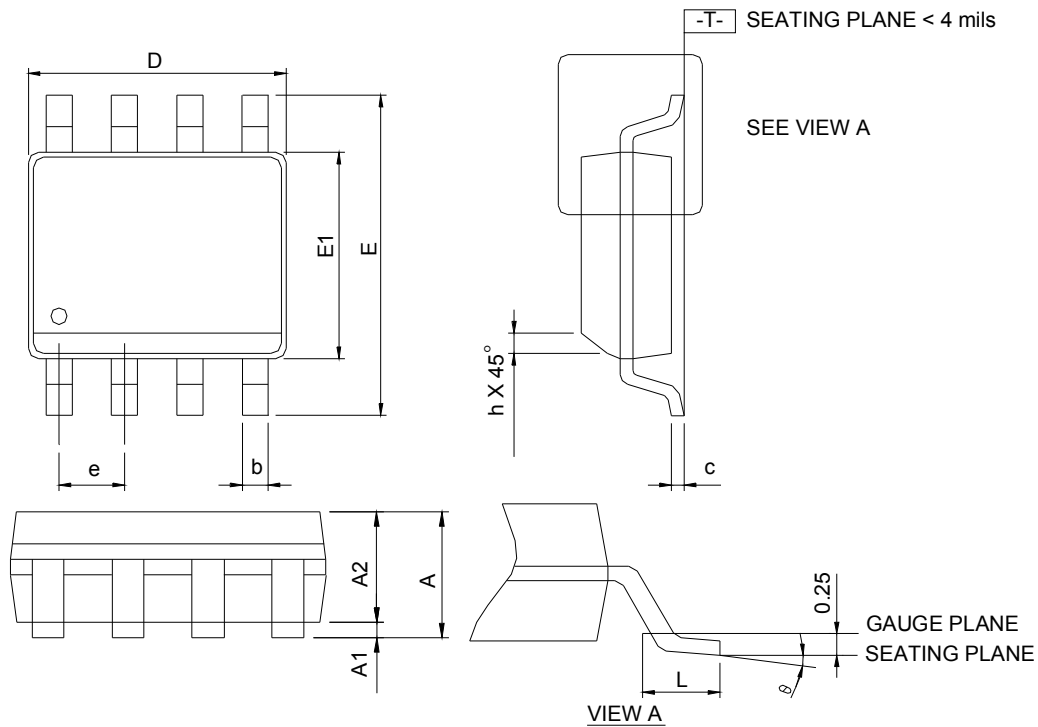


Switching Time Test Circuit and Waveforms



Package Information

SOP-8



DIMENSION	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

