Features

- **N Channel**

  100V/8.8A,

  $R_{DS(ON)}$ = 100mΩ (typ.) @ V_{GS} = 10V

  $R_{DS(ON)}$ = 110mΩ (typ.) @ V_{GS} = 4.5V

- **P Channel**

  -100V/-4.8A,

  $R_{DS(ON)}$ = 150mΩ (typ.) @ V_{GS} =-10V

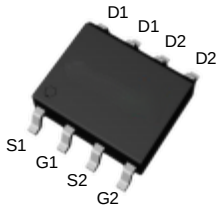
  $R_{DS(ON)}$ = 170mΩ (typ.) @ V_{GS} =-4.5V

- 100% UIS Tested
- Reliable and Rugged
- Lead Free Available (RoHS Compliant)

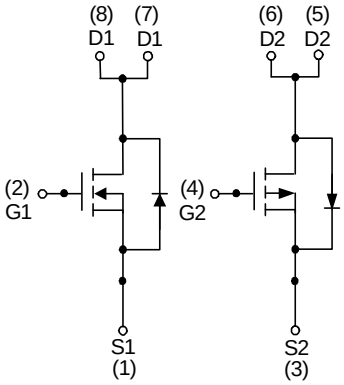
Applications

- Fan Motor Control.
- Synchronous Rectification.

Pin Description



Top View of SOP–8



N-Channel MOSFET P-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C unless otherwise noted)

Symbol	Parameter		N Channel	P Channel	Unit
Common Ratings					
V_{DSS}	Drain-Source Voltage		100	-100	V
V_{GSS}	Gate-Source Voltage		±20		
T_J	Maximum Junction Temperature		150		°C
T_{STG}	Storage Temperature Range		-55 to 150		
I_S	Diode Continuous Forward Current	T_A=25°C	2	-1	A
I_D	Continuous Drain Current	T_A=25°C	8.8	-4.8	A
		T_A=70°C	6	-2.4	
I_{DM} [a]	Pulsed Drain Current	T_A=25°C	10	-7	A
P_D [d]	Maximum Power Dissipation	T_A=25°C	2.1	2.1	W
		T_A=70°C	1.3	1.3	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	t ≤ 10s	60		°C/W
		Steady State [b]	95		°C/W
I_{AS} [c]	Avalanche Current, Single pulse	L=0.5mH	5	-7	A
E_{AS} [c]	Avalanche Energy, Single pulse	L=0.5mH	6.25	12	mJ

Note a：Pulse width limited by max. junction temperature.
Note b：$R_{\theta JA}$ steady state t=100s. $R_{\theta JA}$ is measured with the device mounted on $1in^2$，FR-4 board with 2oz. Copper.
Note c：UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature T_j=25°C).
Note d：t < 10s.

N Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	N Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=80V, V_{GS}=0V	-	-	1	μA
		T_J=85°C	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	1.2	2	2.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$ [e]	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=2.5A	-	100	115	mΩ
		V_{GS}=4.5V, I_{DS}=2A	-	110	138	mΩ
Diode Characteristics						
V_{SD} [e]	Diode Forward Voltage	I_{SD}=2A, V_{GS}=0V	-	0.8	1.3	V
t_{rr}	Reverse Recovery Time	I_{SD}=2.5A, dI_{SD}/dt=100A/μs	-	23	-	ns
Q_{rr}	Reverse Recovery Charge		-	26	-	nC
Dynamic Characteristics [f]						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V,f=1MHz	-	3	6	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, Frequency=1.0MHz	-	440	570	pF
C_{oss}	Output Capacitance		-	30	-	
C_{rss}	Reverse Transfer Capacitance		-	16	-	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=30V, R_L=30Ω, I_{DS}=1A, V_{GEN}=10V, R_G=6Ω	-	6	11	ns
t_r	Turn-on Rise Time		-	6	11	
$t_{d(OFF)}$	Turn-off Delay Time		-	18	33	
t_f	Turn-off Fall Time		-	5	9	
Gate Charge Characteristics [f]						
Q_g	Total Gate Charge	V_{DS}=30V, V_{GS}=4.5V, I_{DS}=2.5A	-	4.8	-	nC
Q_g	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_{DS}=2.5A	-	10	14	
Q_{gs}	Gate-Source Charge		-	2	-	
Q_{gd}	Gate-Drain Charge		-	2	-	

Note e：Pulse test ; pulse width≤300μs, duty cycle≤2%.

Note f：Guaranteed by design, not subject to production testing.

P Channel Electrical Characteristics (T_A = 25°C unless otherwise noted)

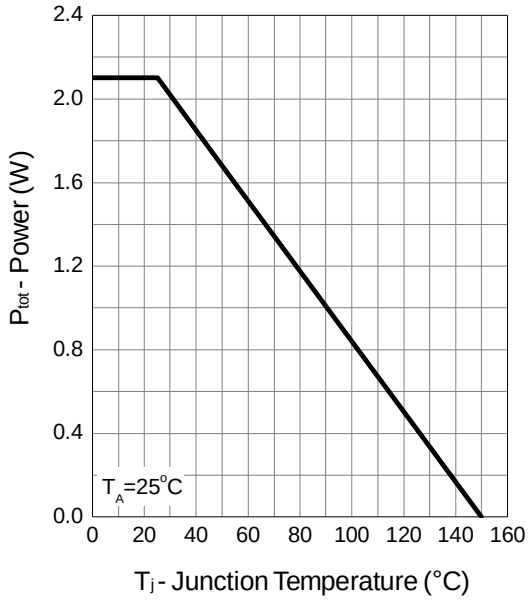
Symbol	Parameter	Test Conditions	P Channel			Unit
			Min.	Typ.	Max.	
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=-250μA	-100	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-80V, V_{GS}=0V	-	-	-1	μA
		T_J=85°C	-	-	-30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=-250μA	-1.2	-1.85	-2.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$ [e]	Drain-Source On-state Resistance	V_{GS}=-10V, I_{DS}=-1.7A	-	150	180	mΩ
		V_{GS}=-4.5V, I_{DS}=-1A	-	170	210	mΩ
Diode Characteristics						
V_{SD} [e]	Diode Forward Voltage	I_{SD}=-1A, V_{GS}=0V	-	-0.75	-1	V
t_{rr}	Reverse Recovery Time	I_{SD}=-1.7A, dI_{SD}/dt=100A/μs	-	28	-	ns
Q_{rr}	Reverse Recovery Charge		-	29	-	nC
Dynamic Characteristics [f]						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V,f=1MHz	-	12	24	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=-30V, Frequency=1.0MHz	-	440	572	pF
C_{oss}	Output Capacitance		-	30	-	
C_{rss}	Reverse Transfer Capacitance		-	17	-	
$t_{d(ON)}$	Turn-on Delay Time	V_{DD}=-30V, R_L=30Ω, I_{DS}=-1A, V_{GEN}=-10V, R_G=6Ω	-	7	13	ns
t_r	Turn-on Rise Time		-	4	7	
$t_{d(OFF)}$	Turn-off Delay Time		-	24	43	
t_f	Turn-off Fall Time		-	23	41	
Gate Charge Characteristics [f]						
Q_g	Total Gate Charge	V_{DS}=-30V, V_{GS}=-4.5V, I_{DS}=-1.7A	-	5.2	-	nC
Q_g	Total Gate Charge	V_{DS}=-30V, V_{GS}=-10V, I_{DS}=-1.7A	-	10.8	16	
Q_{gs}	Gate-Source Charge		-	1.5	-	
Q_{gd}	Gate-Drain Charge		-	2	-	

Note e：Pulse test ; pulse width≤300μs, duty cycle≤2%.

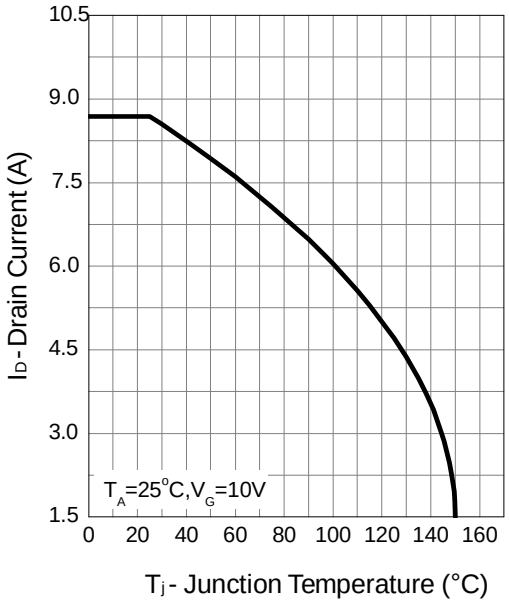
Note f：Guaranteed by design, not subject to production testing.

N Channel Typical Operating Characteristics

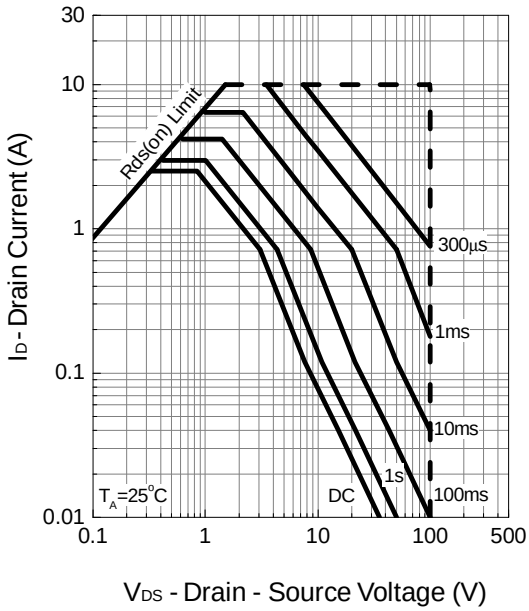
Power Dissipation



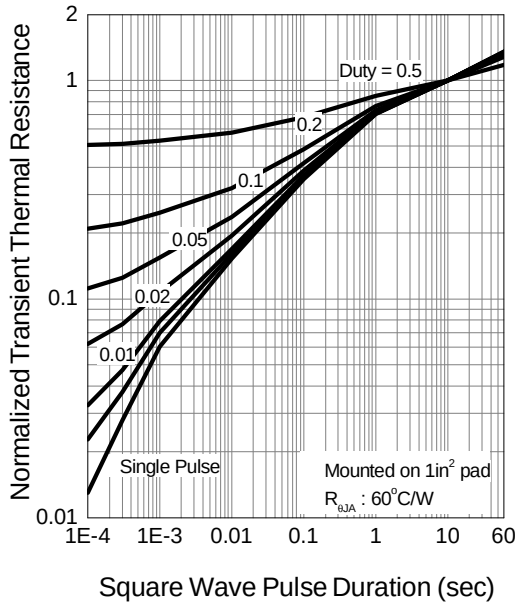
Drain Current



Safe Operation Area

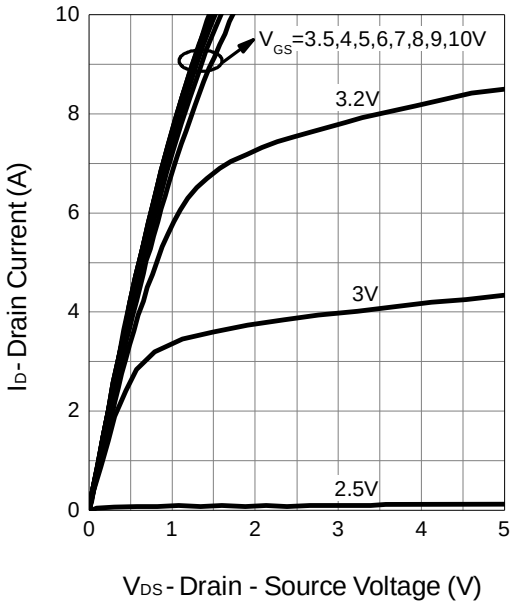


Thermal Transient Impedance

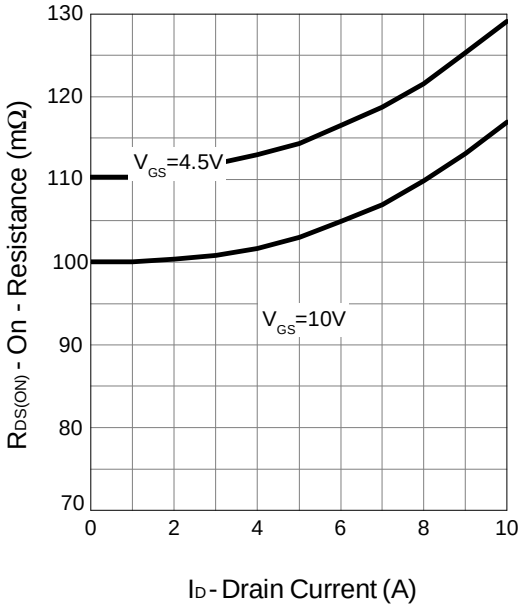


N Channel Typical Operating Characteristics (Cont.)

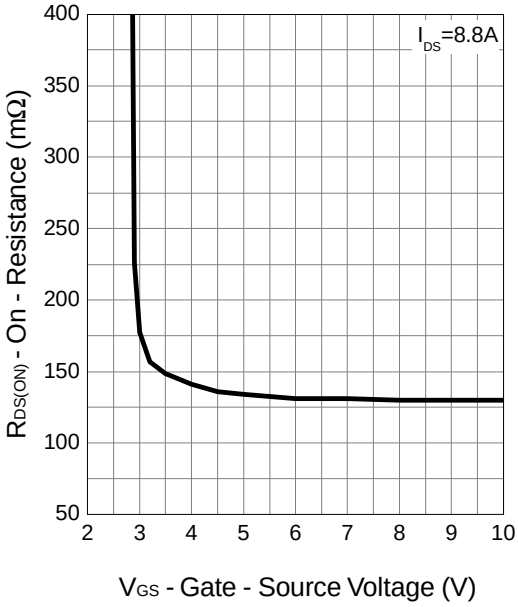
Output Characteristics



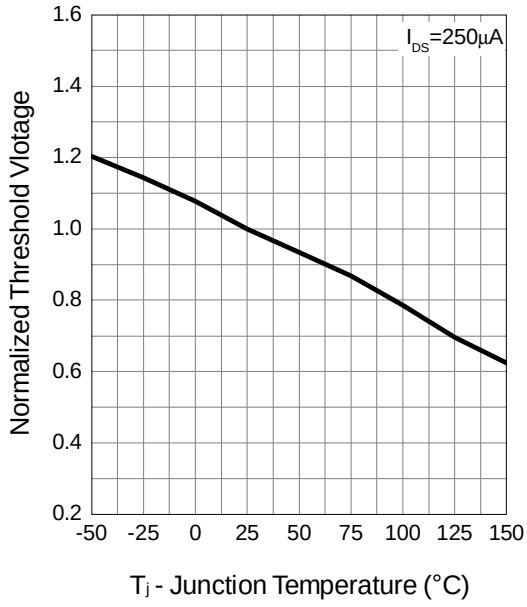
Drain-Source On Resistance



Gate-Source On Resistance

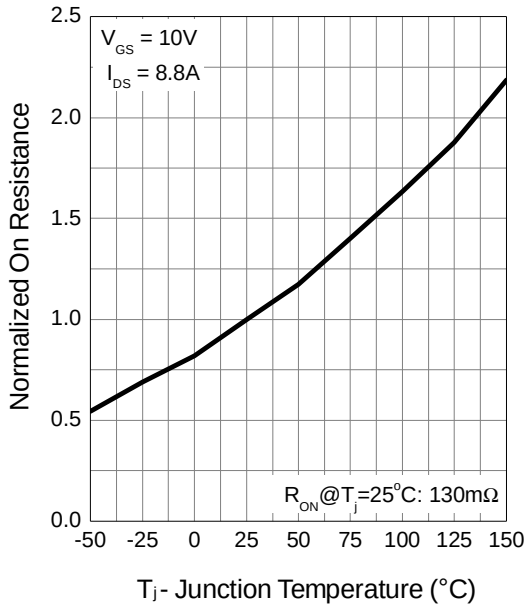


Gate Threshold Voltage

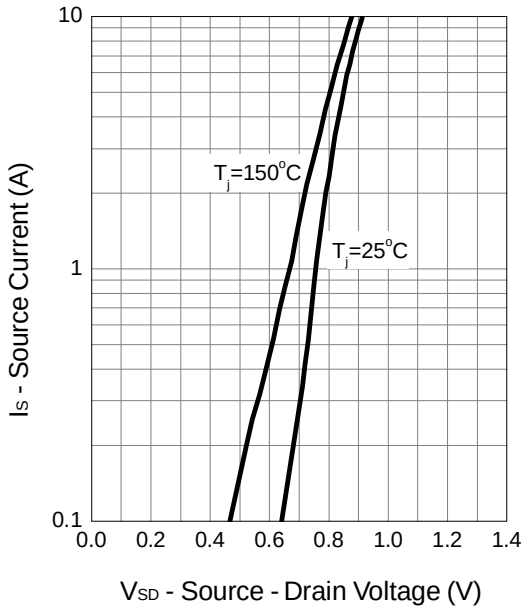


N Channel Typical Operating Characteristics (Cont.)

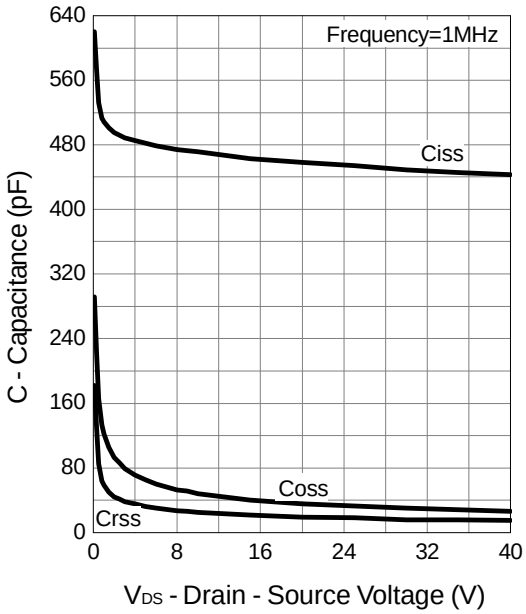
Drain-Source On Resistance



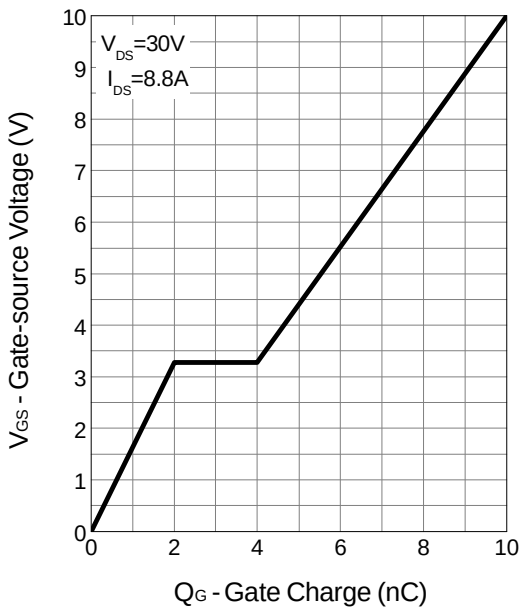
Source-Drain Diode Forward



Capacitance

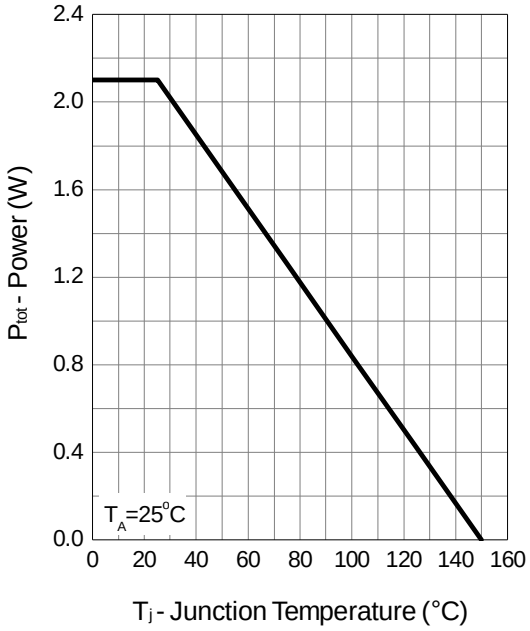


Gate Charge

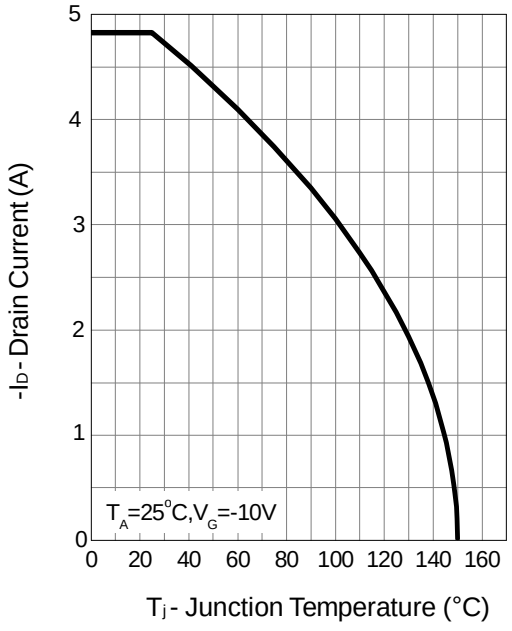


P Channel Typical Operating Characteristics

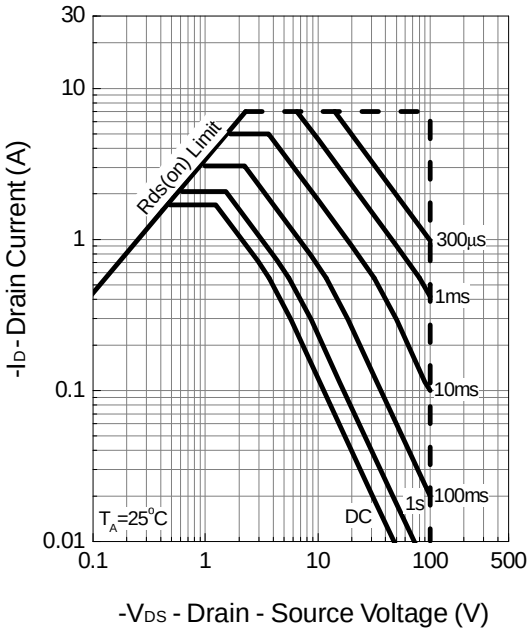
Power Dissipation



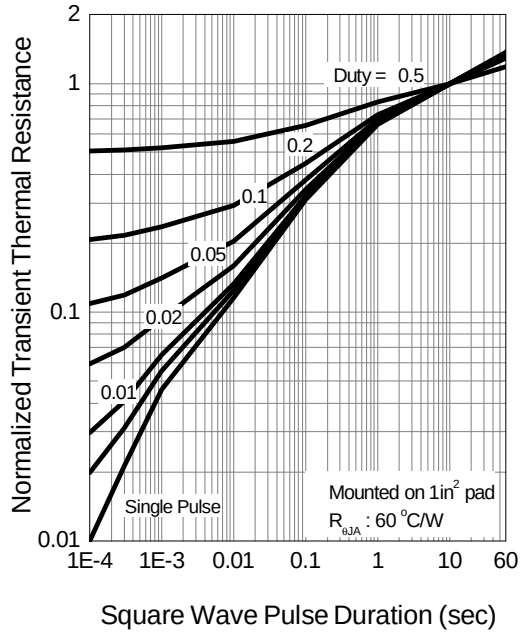
Drain Current



Safe Operation Area

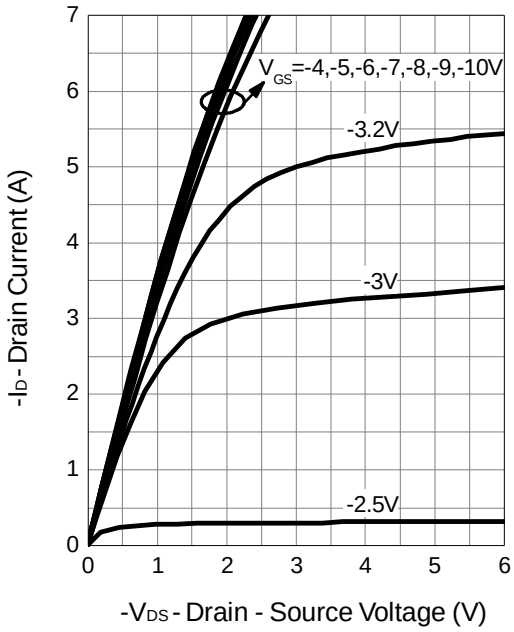


Thermal Transient Impedance

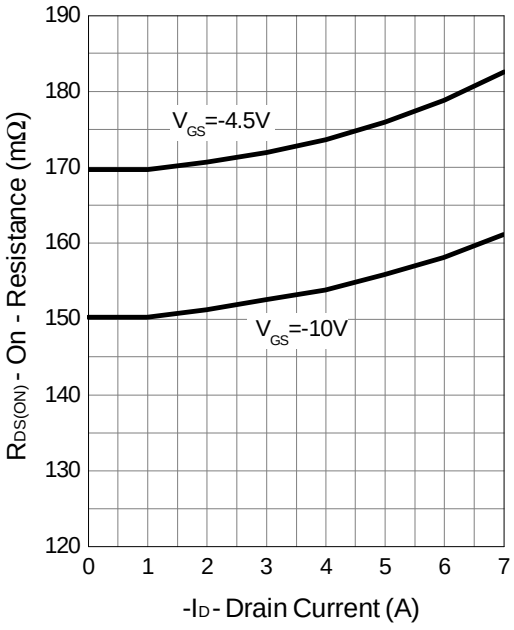


P Channel Typical Operating Characteristics (Cont.)

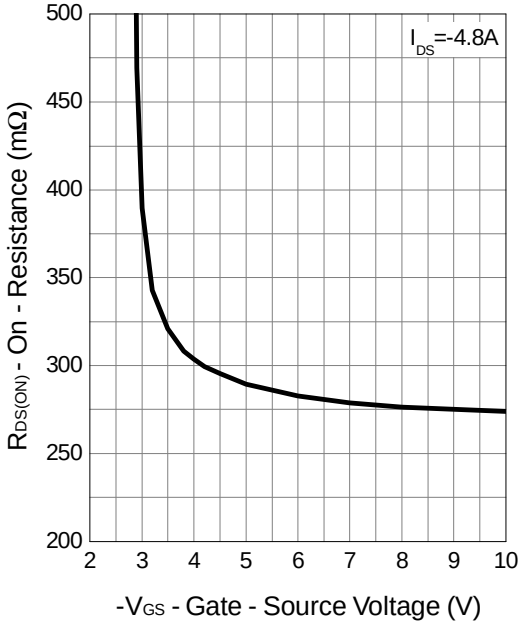
Output Characteristics



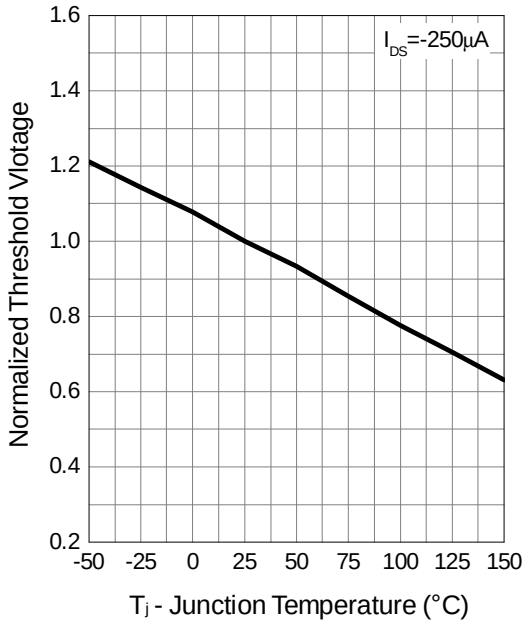
Drain-Source On Resistance



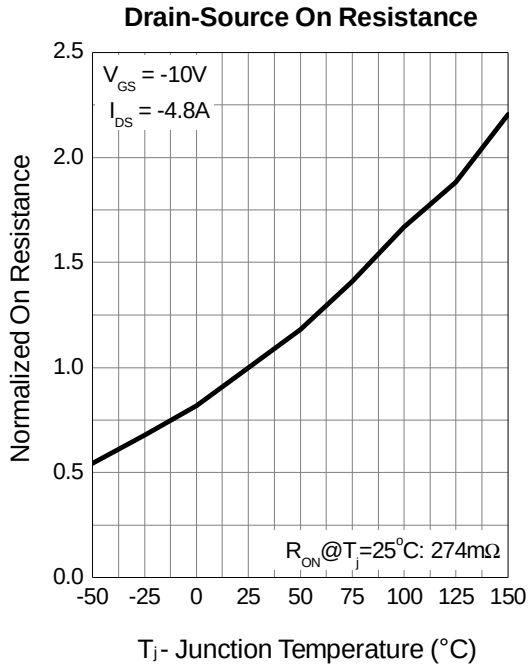
Gate-Source On Resistance

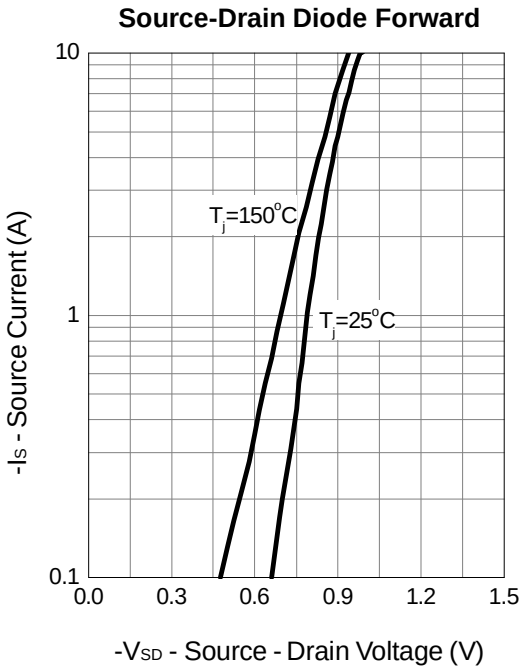


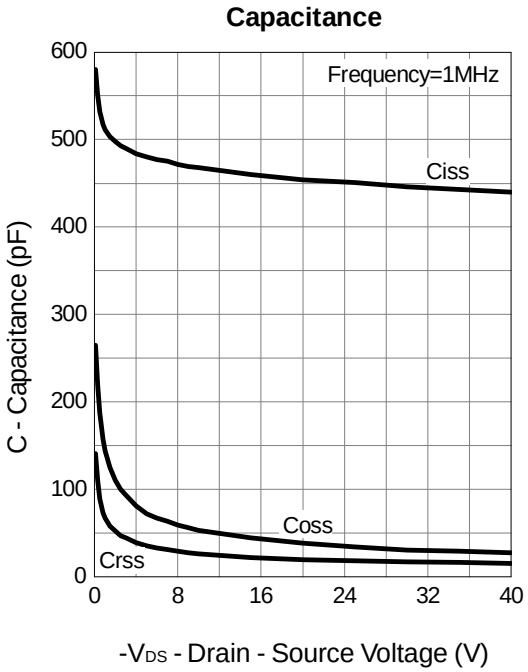
Gate Threshold Voltage

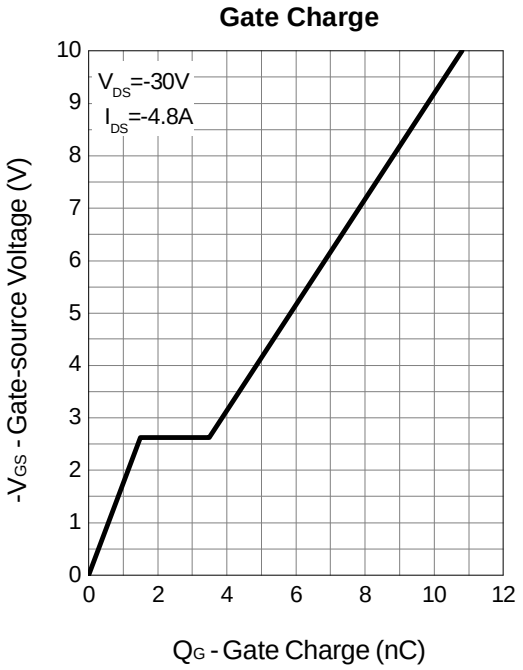


P Channel Typical Operating Characteristics (Cont.)



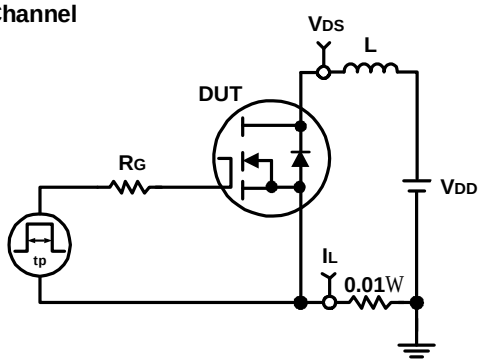


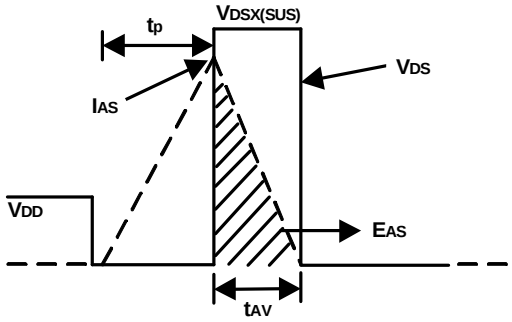




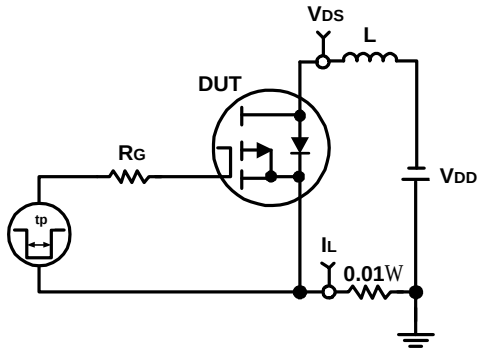
Avalanche Test Circuit and Waveforms

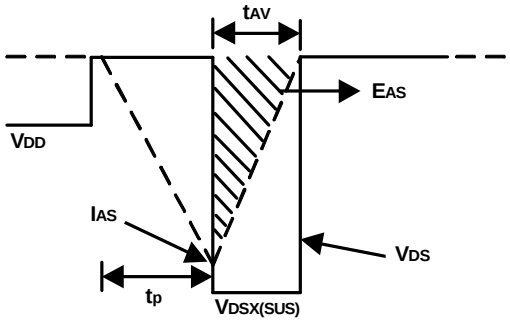
N Channel





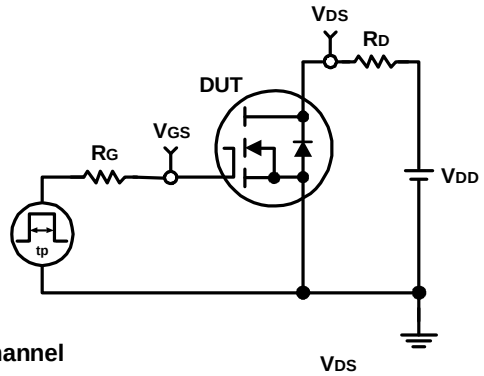
P Channel

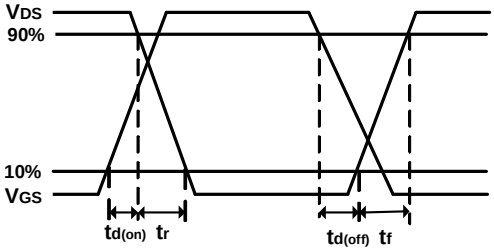




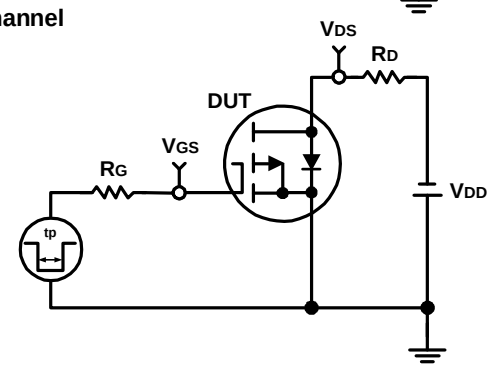
Switching Time Test Circuit and Waveforms

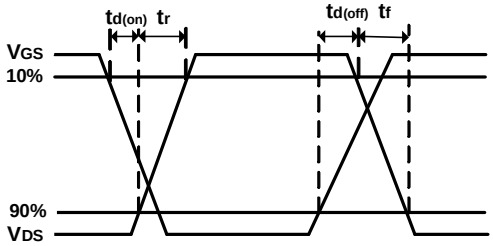
N Channel





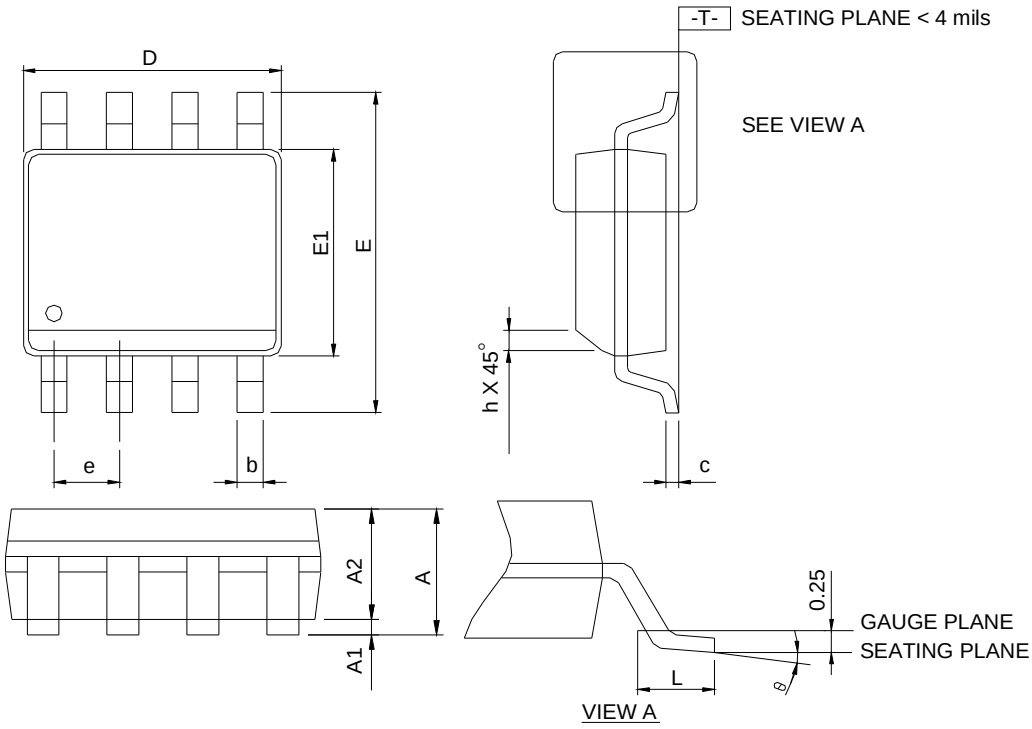
P Channel





Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN