

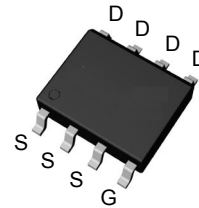
Features

- -40V/-11A,
 $R_{DS(ON)} = 13m\Omega$ (typ.) @ $V_{GS} = -10V$
 $R_{DS(ON)} = 18m\Omega$ (typ.) @ $V_{GS} = -4.5V$
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

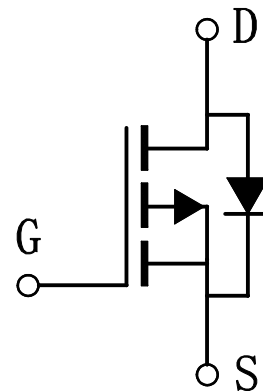
Applications

- Power Management in Desktop Computer or DC/DC Converters.
- Power Load Switch.
- Notebook Battery Management.

Pin Description



Top View of SOP8



P-Channel MOSFET

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	-40	V
V_{GSS}	Gate-Source Voltage	± 25	
I_D^a	Continuous Drain Current ($V_{GS} = -10V$)	$T_A = 25^\circ C$	A
		$T_A = 70^\circ C$	
I_{DM}^a	300 μs Pulsed Drain Current ($V_{GS} = -10V$)	-44	
I_S^a	Diode Continuous Forward Current	-3	
I_{AS}^b	Avalanche Current, Single pulse ($L = 0.1mH$)	-33	
E_{AS}^b	Avalanche Energy, Single pulse ($L = 0.1mH$)	54	mJ
T_J	Maximum Junction Temperature	150	$^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150	
P_D^a	Maximum Power Dissipation	$T_A = 25^\circ C$	W
		$T_A = 70^\circ C$	
$R_{\theta JA}^a$	Thermal Resistance-Junction to Ambient	$t \leq 10s$	$^\circ C/W$
		Steady State	
$R_{\theta JL}^c$	Thermal Resistance-Junction to Lead	Steady State	

Note a: Surface Mounted on 1in² pad area, $t \leq 10sec$.

Note b: UIS tested and pulse width limited by maximum junction temperature 150 $^\circ C$ (initial temperature $T_J = 25^\circ C$).

Note c: The power dissipation P_D is based on $T_{J(MAX)} = 150^\circ C$, and it is useful for reducing junction-to-case thermal resistance ($R_{\theta JC}$) when additional heat sink is used.

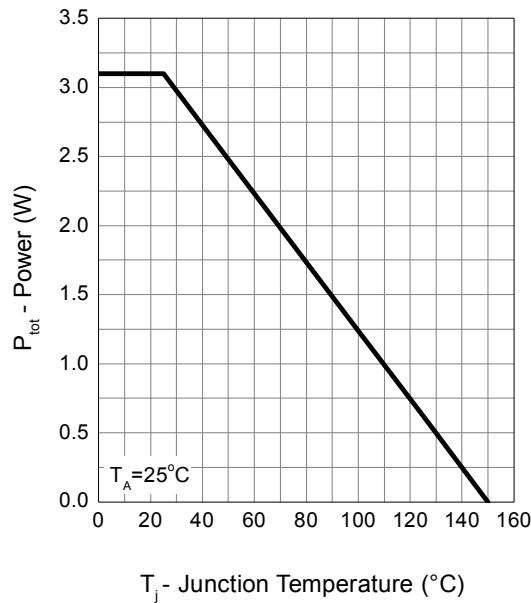
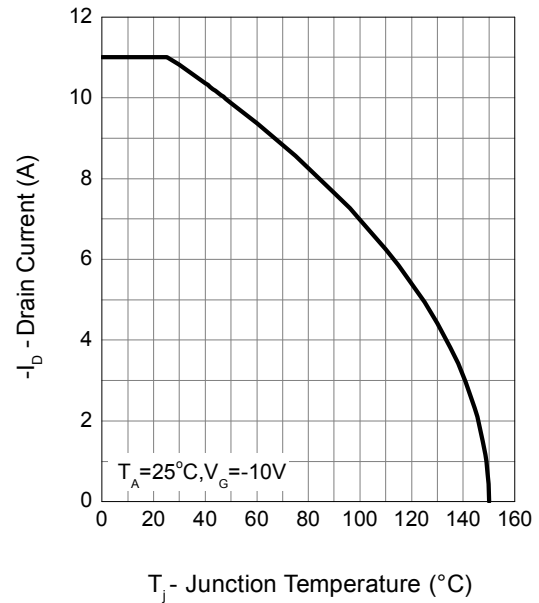
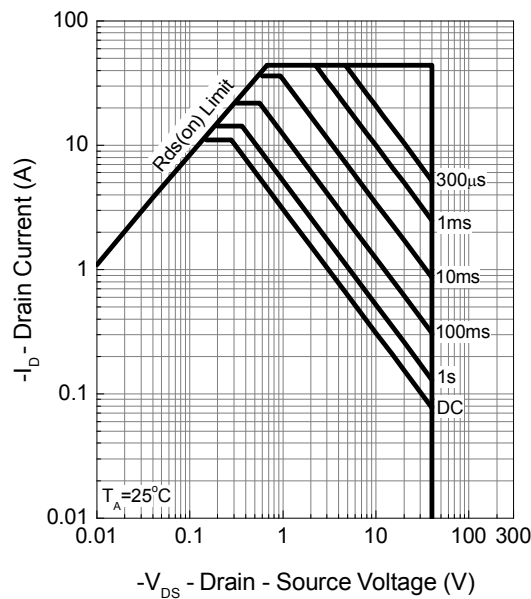
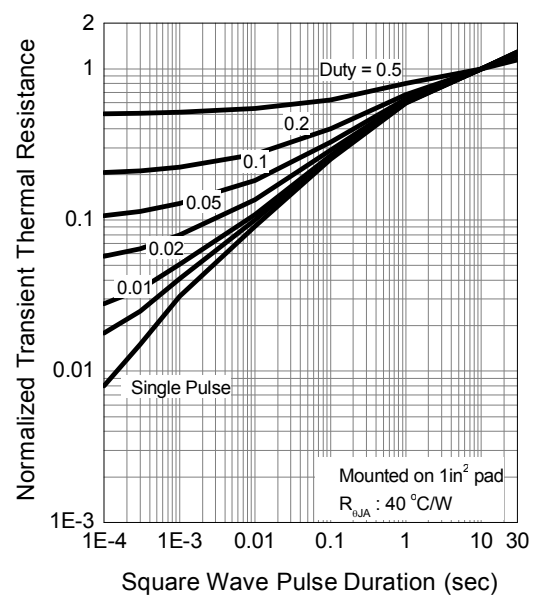
Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250μA	-40	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-32V, V _{GS} =0V T _J =85°C	-	-	-1 -30	μA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250μA	-1.4	-1.9	-2.4	V
I _{GSS}	Gate Leakage Current	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^a	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-11A V _{GS} =-4.5V, I _{DS} =-7A	-	13 18	16 22	mΩ
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =-1A, V _{GS} =0V	-	-0.75	-1	V
t _{rr}	Reverse Recovery Time	I _{SD} =-11A, dI _{SD} /dt=100A/μs	-	24	-	ns
Q _{rr}	Reverse Recovery Charge		-	18	-	nC
Dynamic Characteristics ^b						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	-	2.3	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-20V, Frequency=1.0MHz	-	1500	-	pF
C _{oss}	Output Capacitance		-	235	-	
C _{rss}	Reverse Transfer Capacitance		-	180	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =-20V, R _L =20Ω, I _{DS} =-1A, V _{GEN} =-10V, R _G =6Ω	-	14	-	ns
t _r	Turn-on Rise Time		-	12	-	
t _{d(OFF)}	Turn-off Delay Time		-	41	-	
t _f	Turn-off Fall Time		-	22	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =-20V, V _{GS} =-10V, I _{DS} =-11A	-	32	-	nC
Q _{gs}	Gate-Source Charge		-	5.2	-	
Q _{gd}	Gate-Drain Charge		-	8	-	

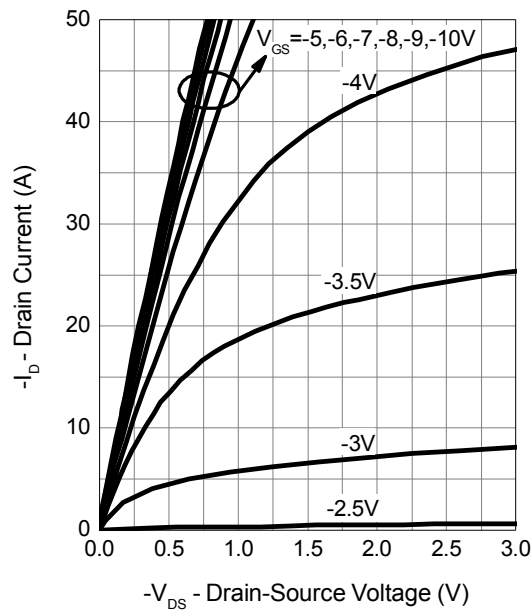
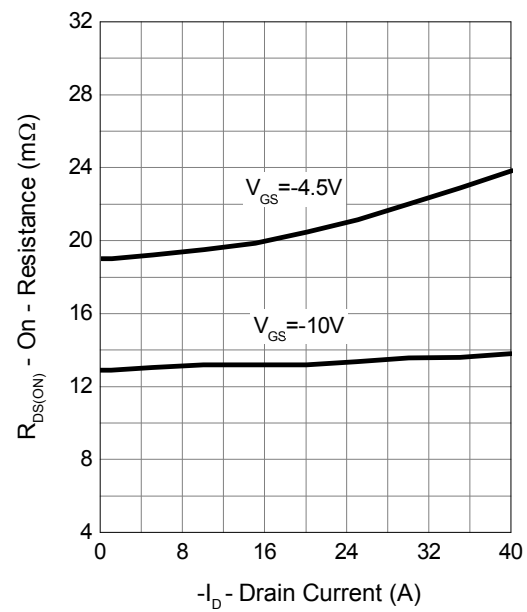
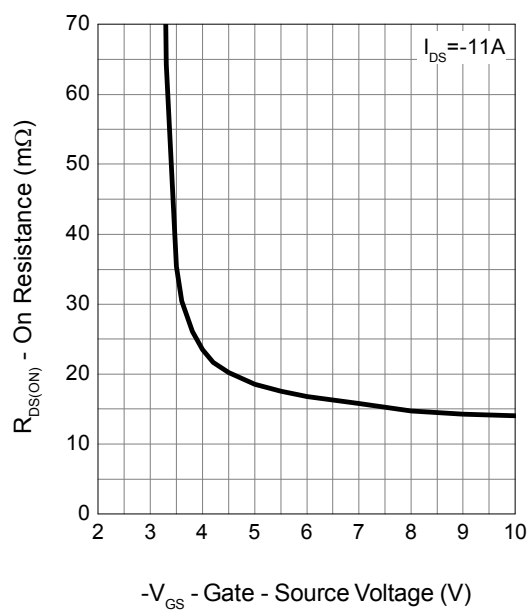
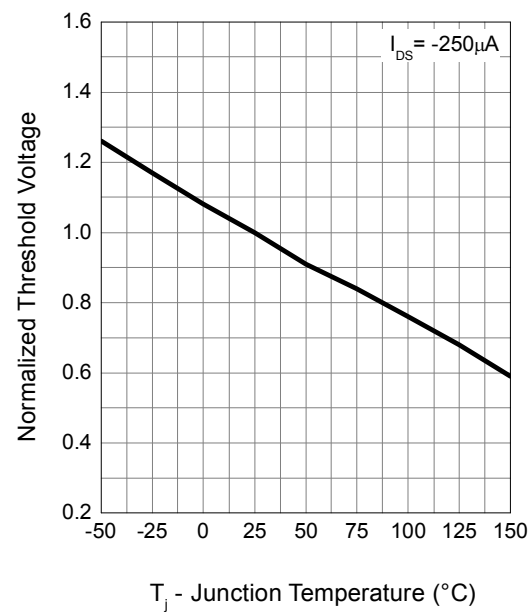
Note a: Pulse test; pulse width≤300μs, duty cycle≤2%.

Note b: Guaranteed by design, not subject to production testing.

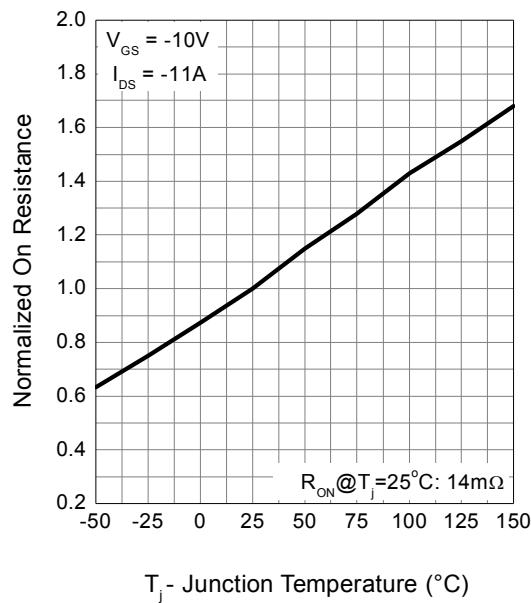
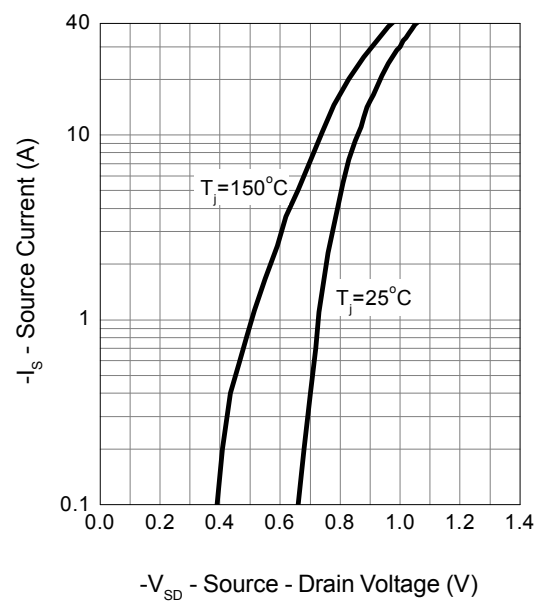
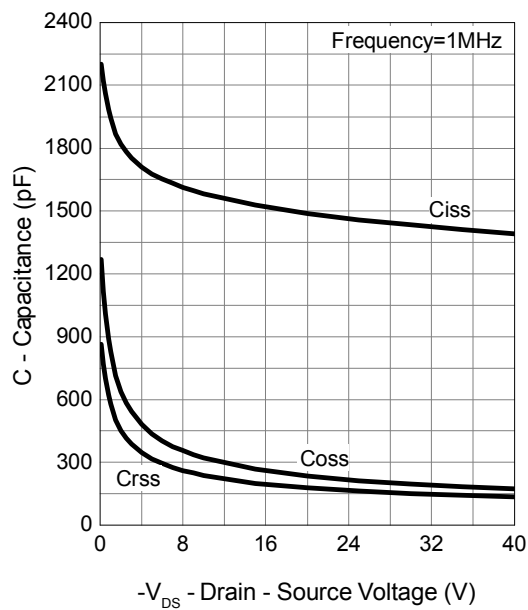
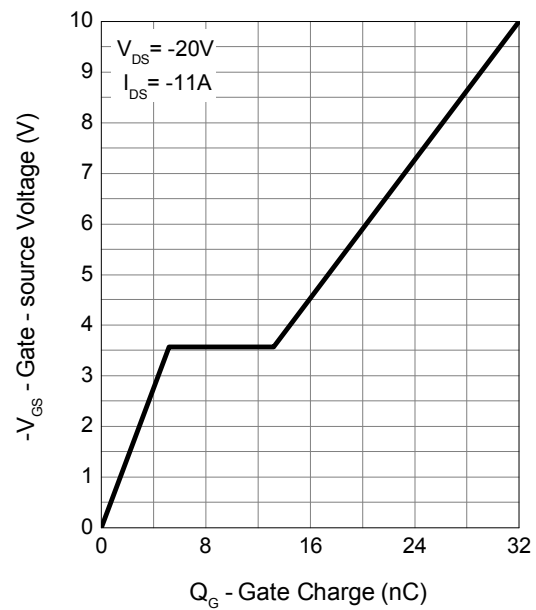
Typical Operating Characteristics

Power Dissipation

Drain Current

Safe Operation Area

Thermal Transient Impedance


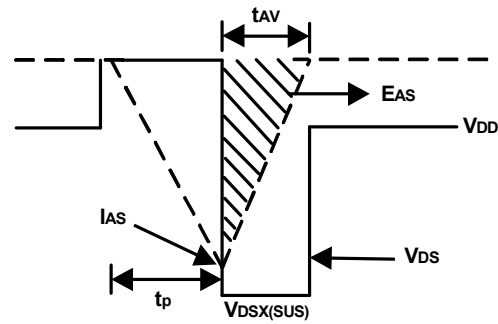
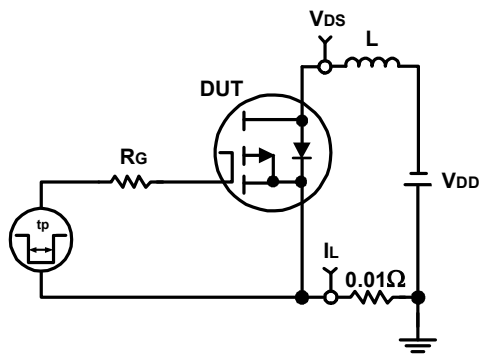
Typical Operating Characteristics (Cont.)

Output Characteristics

Drain-Source On Resistance

Gate-Source On Resistance

Gate Threshold Voltage


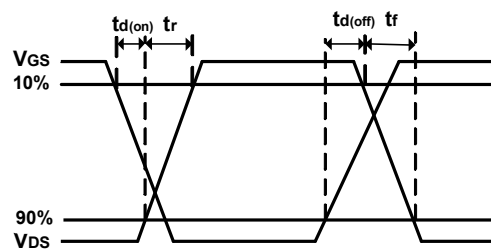
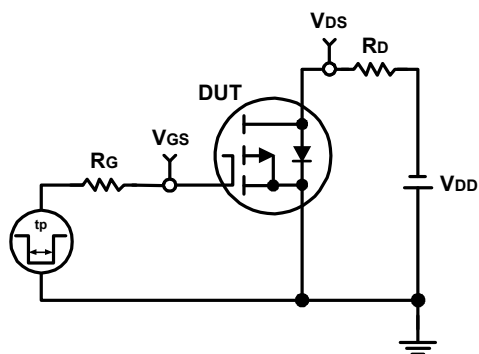
Typical Operating Characteristics (Cont.)

Drain-Source On Resistance

Source-Drain Diode Forward

Capacitance

Gate Charge


Avalanche Test Circuit and Waveforms

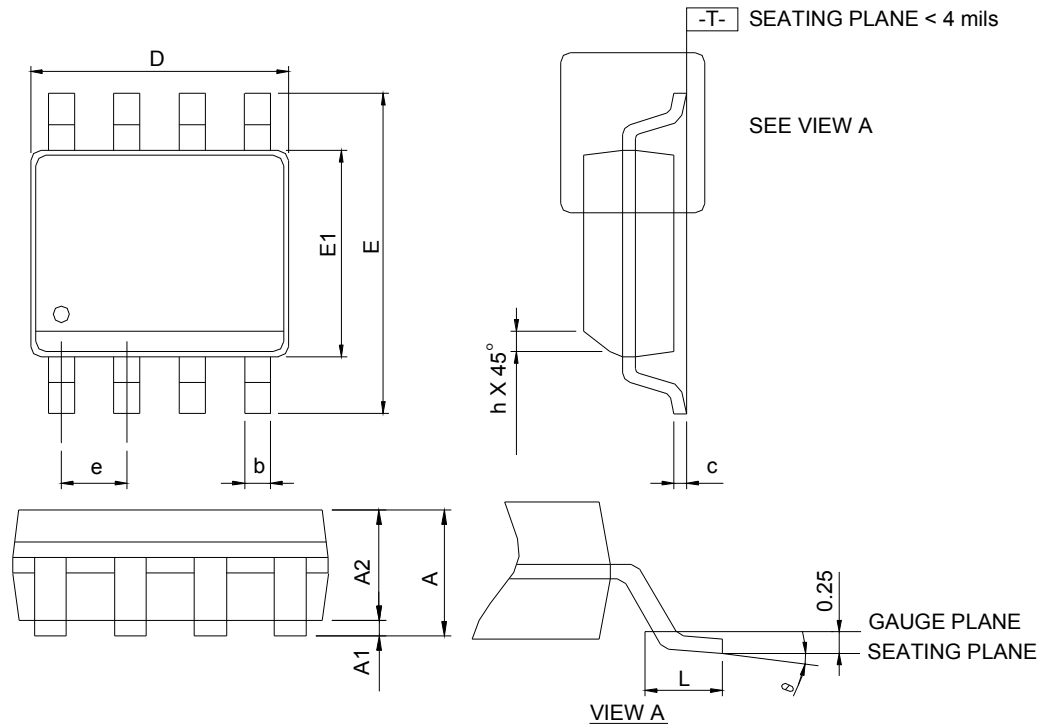


Switching Time Test Circuit and Waveforms



Package Information

SOP8



DIMENSIONS	SOP8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

