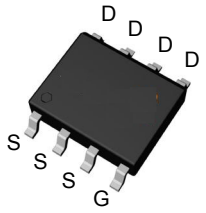
## Features

- -60V/-4.6A,
  $R_{DS(ON)}$ = 64mΩ(typ.) @ $V_{GS}$ =-10V
  $R_{DS(ON)}$ = 105mΩ(typ.) @ $V_{GS}$ =-4.5V
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

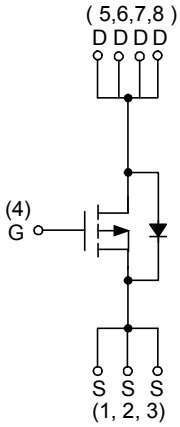
## Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

## Pin Description




Top View of SOP-8




P-Channel MOSFET

### Maximum ratings, at $T_A$ =25 °C, unless otherwise specified

| Symbol | Parameter | | Rating | Unit |
|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-Source breakdown voltage | | -60 | V |
| $I_S$ | Diode continuous forward current | $T_A$ =25°C | -4.6 | A |
| $I_D$ | Continuous drain current@$V_{GS}$=10V | $T_A$ =25°C | -4.6 | A |
| | | $T_A$ =100°C | -3.45 | A |
| $I_{DM}$ | Pulse drain current tested ② | $T_A$ =25°C | -13.2 | A |
| $P_D$ | Power dissipation | $T_A$ =25°C | 3.1 | W |
| VGS | Gate-Source voltage | | ±20 | V |
| $T_{STG}$ | Storage temperature range | | -55 to 150 | °C |
| $T_J$ | Maximum Junction Temperature① | | 150 | °C |
| $R_{\theta JC}$ | Thermal Resistance-Junction to Case | | 24 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance Junction-Ambient | | 40 | °C/W |

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static Electrical Characteristics @ $T_A$ = 25°C (unless otherwise stated)** | | | | | | |
| $V_{(BR)DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V $I_D$=-250μA | -60 | -- | -- | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current($T_A$=25℃) | $V_{DS}$=-60V,$V_{GS}$=0V | -- | -- | -1 | μA |
| | Zero Gate Voltage Drain Current($T_A$=125℃) | $V_{DS}$=-60V,$V_{GS}$=0V | -- | -- | -100 | μA |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$=±20V,$V_{DS}$=0V | -- | -- | ±100 | nA |
| $V_{GS(TH)}$ | Gate Threshold Voltage | $V_{DS}$=$V_{GS}$,$I_D$=-250μA | -1.0 | -1.7 | -3.0 | V |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance② | $V_{GS}$=-10V, $I_D$=-4A | -- | 64 | 70 | mΩ |
| $R_{DS(ON)}$ | Drain-Source On-State Resistance② | $V_{GS}$=-4.5V, $I_D$=-2A | -- | 105 | 115 | mΩ |
| **Dynamic Electrical Characteristics @ $T_A$= 25°C (unless otherwise stated)** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$=-30V,$V_{GS}$=0V, f=1MHz | -- | 940 | -- | pF |
| $C_{oss}$ | Output Capacitance | | -- | 55 | -- | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | -- | 40 | -- | pF |
| $Q_g$ | Total Gate Charge | $V_{DS}$=-30V,$I_D$=-4A, $V_{GS}$=-10V | -- | 17.5 | -- | nC |
| $Q_{gs}$ | Gate-Source Charge | | -- | 2.8 | -- | nC |
| $Q_{gd}$ | Gate-Drain Charge | | -- | 3.6 | -- | nC |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-on Delay Time | $V_{DD}$=-30V, $I_D$=-4A, $R_G$=6.8Ω, $V_{GS}$=-10V | -- | 9 | -- | nS |
| $t_r$ | Turn-on Rise Time | | -- | 4 | -- | nS |
| $t_{d(off)}$ | Turn-Off Delay Time | | -- | 33 | -- | nS |
| $t_f$ | Turn-Off Fall Time | | -- | 8 | -- | nS |
| **Source- Drain Diode Characteristics@ $T_A$ = 25°C (unless otherwise stated)** | | | | | | |
| $V_{SD}$ | Forward on voltage | $I_{SD}$=-4A,$V_{GS}$=0V | -- | -0.85 | -1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $T_j$=25℃,$I_{sd}$=-4A, $V_{GS}$=0V di/dt=-100A/μs | -- | 32 | -- | nS |
| $Q_{rr}$ | Reverse Recovery Charge | | -- | 39 | -- | nC |

NOTE:

① Repetitive rating; pulse width limited by max. junction temperature.

②Pulse width ≤ 300μs; duty cycle≤ 2%.

## Typical Characteristics

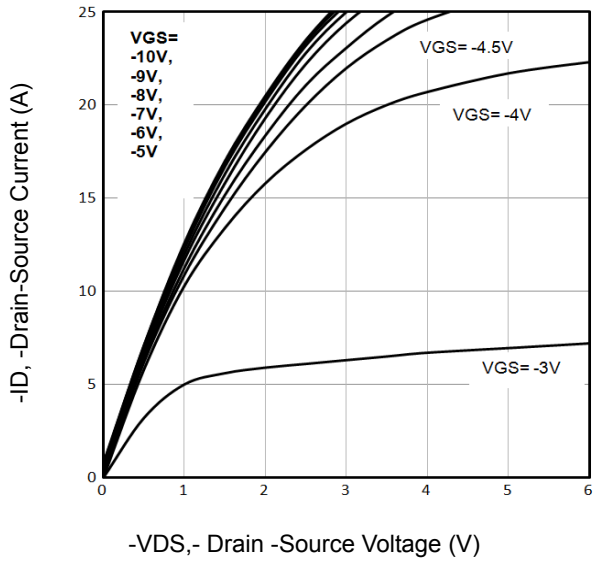



**Fig1.** Typical Output Characteristics

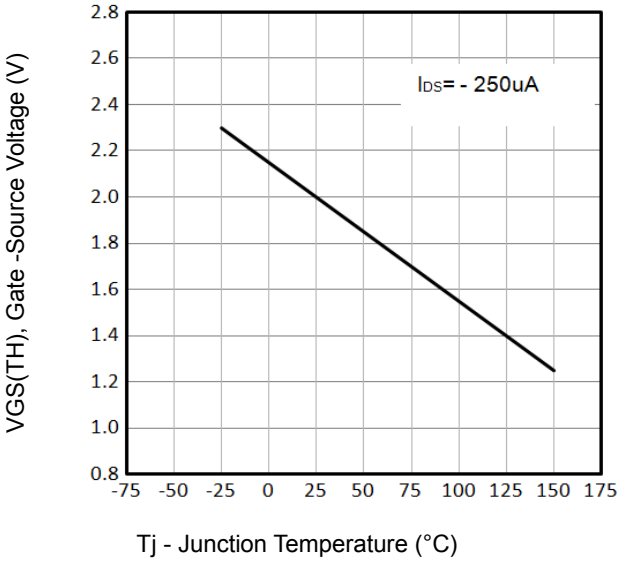



**Fig2.** $V_{GS(TH)}$ Gate -Source Voltage Vs.Tj

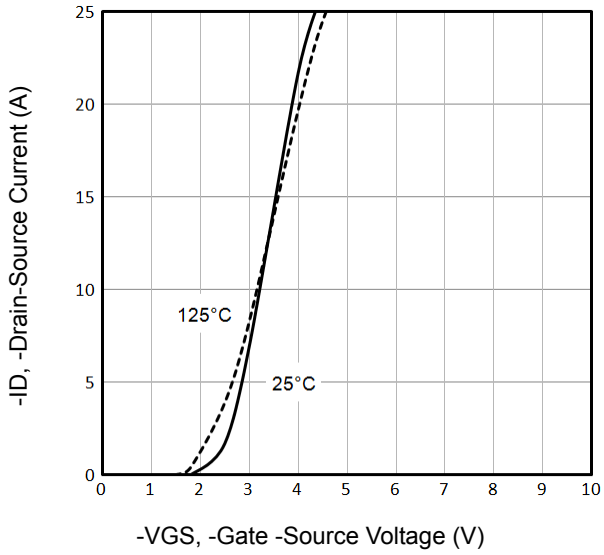



**Fig3.** Typical Transfer Characteristics

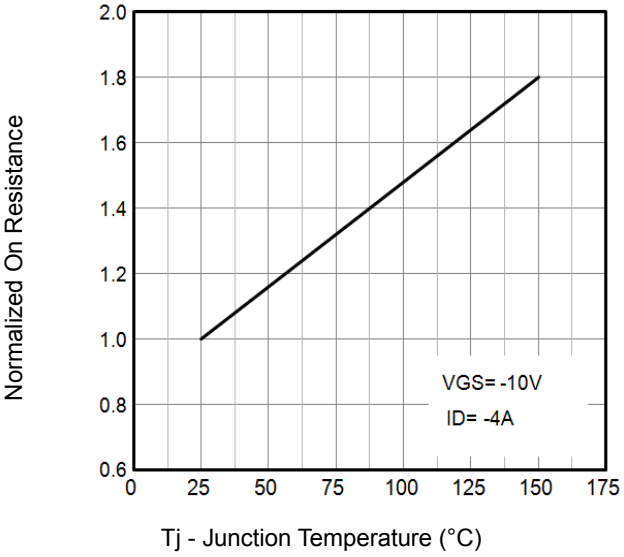



**Fig4.** Normalized On-Resistance Vs. Tj

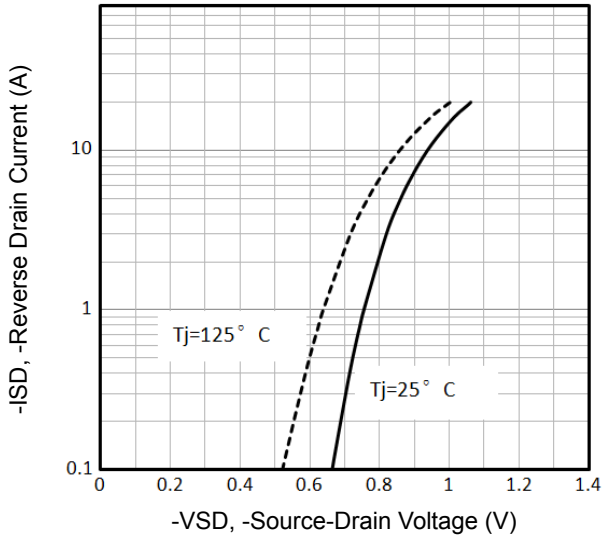



**Fig5.** Typical Source-Drain Diode Forward Voltage

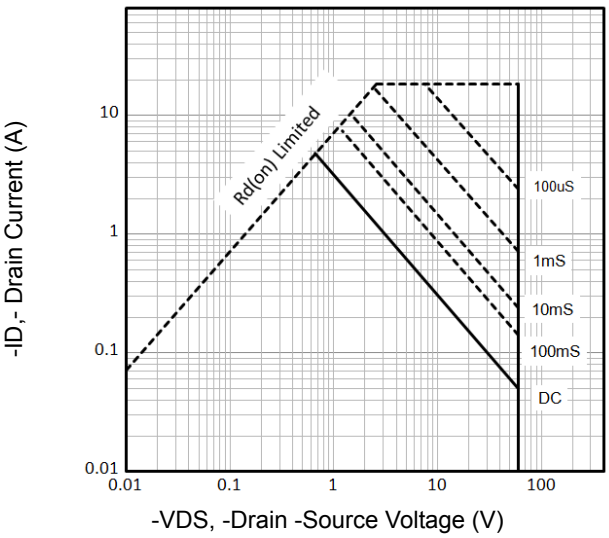



**Fig6.** Maximum Safe Operating Area

## Typical Characteristics

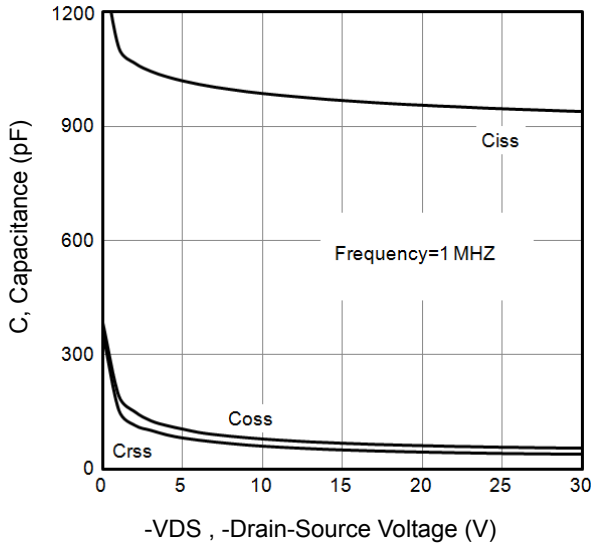



**Fig7.** Typical Capacitance Vs.Drain-Source Voltage

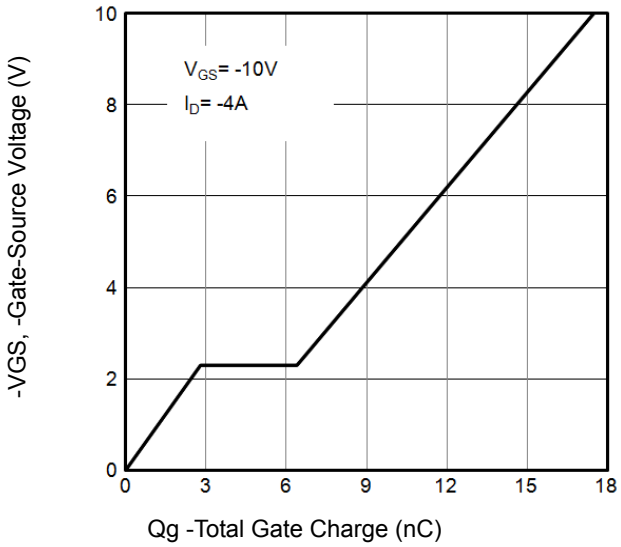



**Fig8.** Typical Gate Charge Vs.Gate-Source Voltage

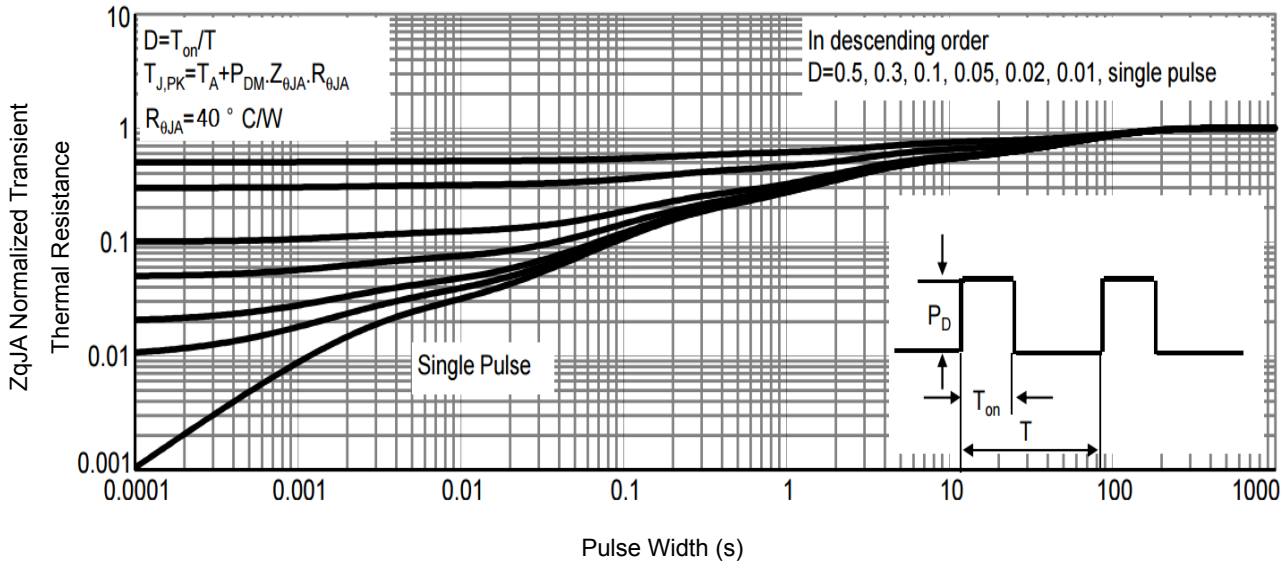
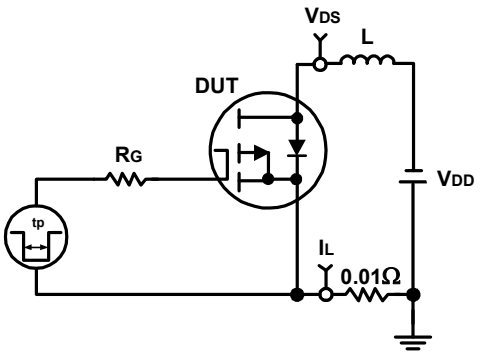
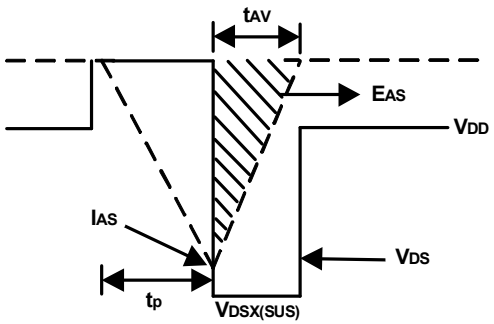


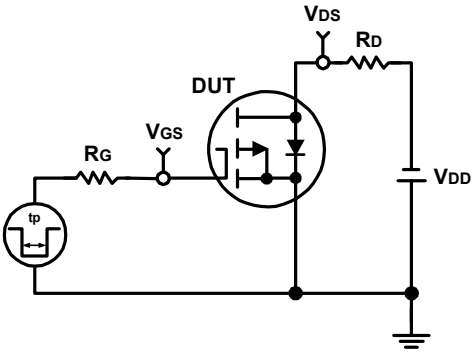

**Fig9.** Normalized Maximum Transient Thermal Impedance

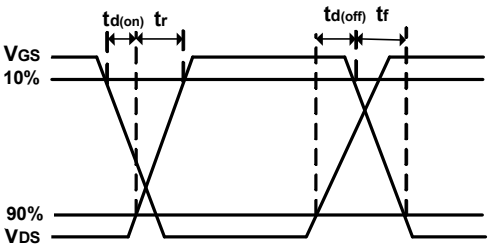
## Avalanche Test Circuit and Waveforms



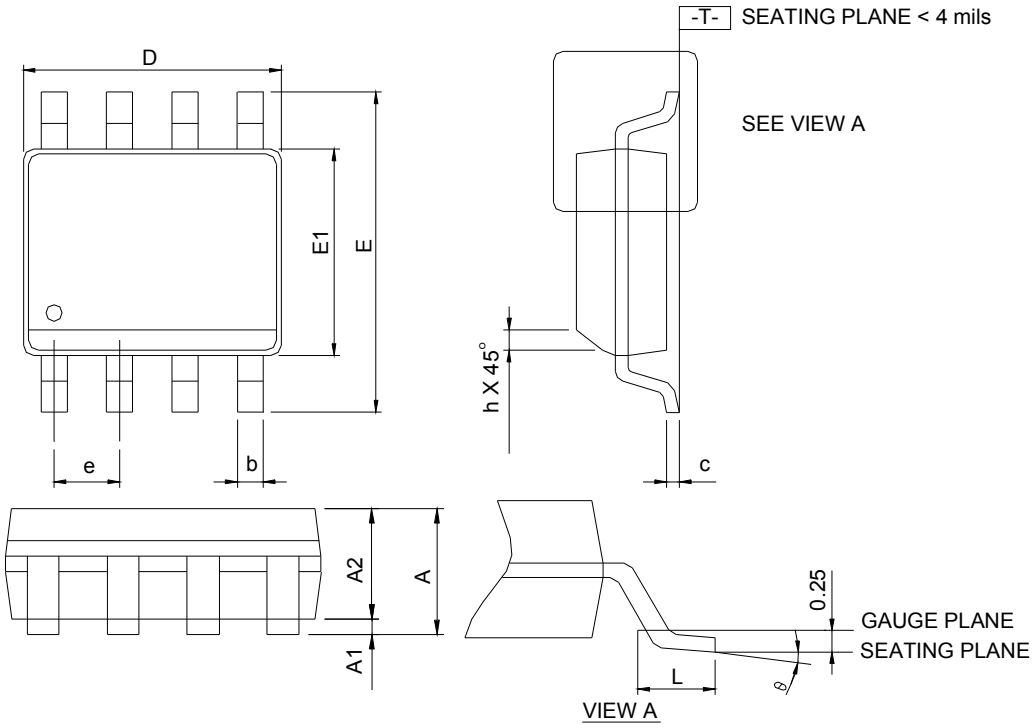

## Switching Time Test Circuit and Waveforms



# Package Information

**SOP-8**




| SYMBOL | SOP-8 | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN. | MAX. | MIN. | MAX. |
| A | - | 1.75 | - | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | 1.25 | - | 0.049 | - |
| b | 0.31 | 0.51 | 0.012 | 0.020 |
| c | 0.17 | 0.25 | 0.007 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.197 |
| E | 5.80 | 6.20 | 0.228 | 0.244 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 BSC | | 0.050 BSC | |
| h | 0.25 | 0.50 | 0.010 | 0.020 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

**RECOMMENDED LAND PATTERN**