

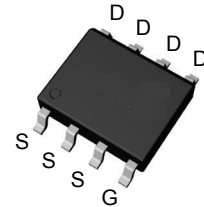
Features

- 30V/20A,
 $R_{DS(ON)} = 4.5m\Omega(Typ.) @ V_{GS} = 10V$
 $R_{DS(ON)} = 6.1m\Omega(Typ.) @ V_{GS} = 4.5V$
- 100% UIS + R_g Tested
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

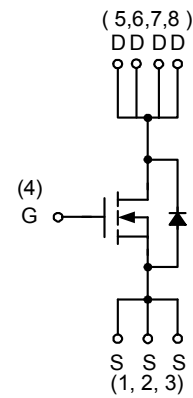
Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

Pin Description



Top View of SOP-8



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter	Rating	Unit
V_{DSS}	Drain-Source Voltage	30	V
V_{GSS}	Gate-Source Voltage	± 20	
I_D^a	Continuous Drain Current ($V_{GS}=10\text{V}$)	$T_A=25^\circ\text{C}$	20
		$T_A=70^\circ\text{C}$	15.8
I_{DM}^a	300 μs Pulsed Drain Current ($V_{GS}=10\text{V}$)	60	A
I_S^a	Diode Continuous Forward Current	20	
I_{AS}^b	Avalanche Current (Single Pulse)	25	
E_{AS}^b	Single Pulse Avalanche Energy ($L=0.1\text{mH}$)	31	mJ
T_J	Maximum Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-55 to 150	
P_D^a	Maximum Power Dissipation	$T_A=25^\circ\text{C}$	4.2
		$T_A=70^\circ\text{C}$	2.6
$R_{\theta JA}^{a,c}$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{s}$	30
		Steady State	65
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	Steady State	20

Note a : Surface Mounted on 1in² pad area, $t \leq 10\text{sec}$.

Note b : UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature $T_J=25^\circ\text{C}$).

Note c : Maximum under Steady State conditions is 75°C/W .

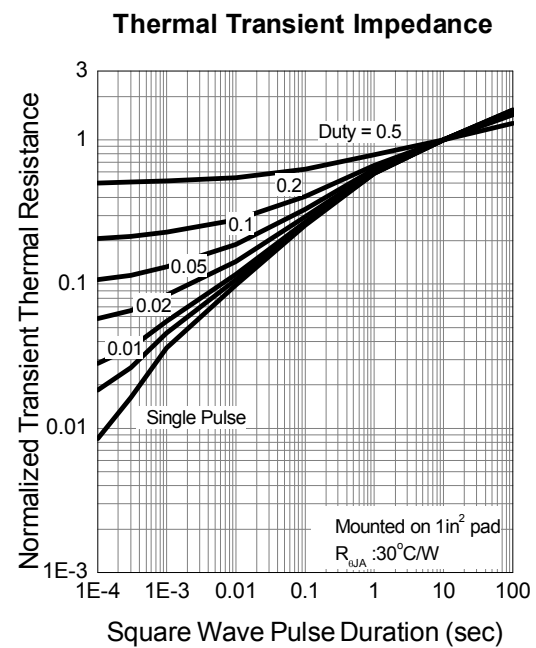
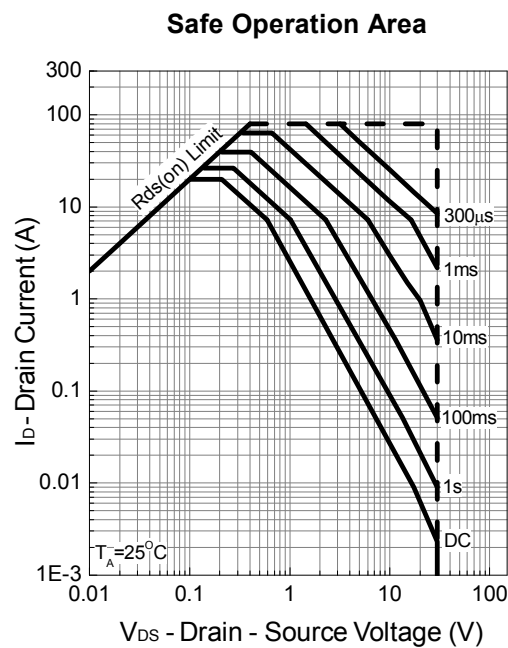
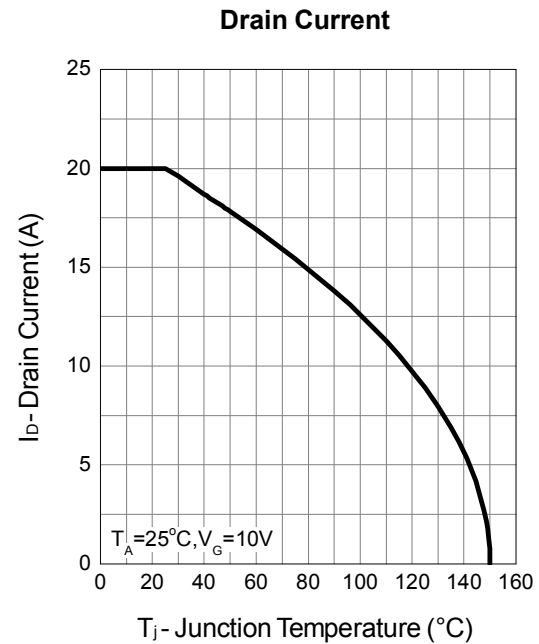
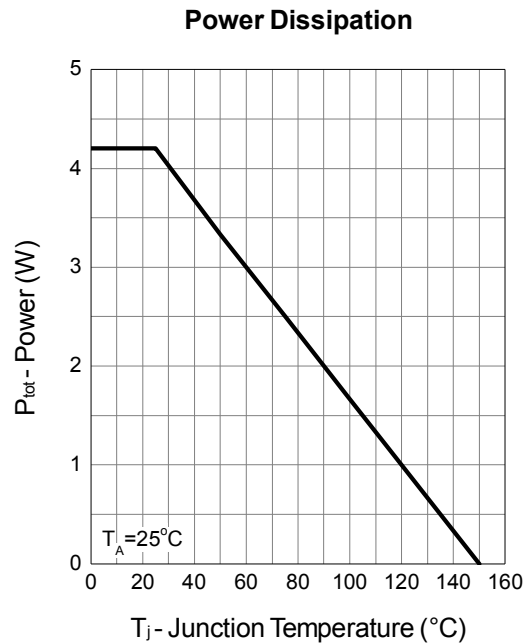
Electrical Characteristics (T_A = 25°C Unless Otherwise Noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V	-	-	1	μA
		T _J =85°C	-	-	30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1.3	1.8	2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^a	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =20A	-	4.5	5.9	mΩ
		V _{GS} =4.5V, I _{DS} =14A	-	6.1	7.9	
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	I _{SD} =5A, V _{GS} =0V	-	0.8	1.1	V
t _{rr} ^b	Reverse Recovery Time	I _{SD} =20A, dI _{SD} /dt=100A/μs	-	10	-	ns
Q _{rr} ^b	Reverse Recovery Charge		-	3	-	nC
Dynamic Characteristics ^b						
R _G	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	-	2.4	-	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =15V, Frequency=1.0MHz	-	1700	-	pF
C _{oss}	Output Capacitance		-	265	-	
C _{rss}	Reverse Transfer Capacitance		-	165	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =15V, R _L =15Ω, I _{DS} =1A, V _{GEN} =10V, R _G =6Ω	-	14	26	ns
t _r	Turn-on Rise Time		-	10	19	
t _{d(OFF)}	Turn-off Delay Time		-	44	80	
t _f	Turn-off Fall Time		-	12	23	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _{DS} =20A	-	28.3	39.6	nC
	Total Gate Charge	V _{DS} =15V, V _{GS} =4.5V, I _{DS} =20A	-	12.9	-	
Q _{gs}	Gate-Source Charge		-	4.22	-	
Q _{gd}	Gate-Drain Charge		-	7.3	-	

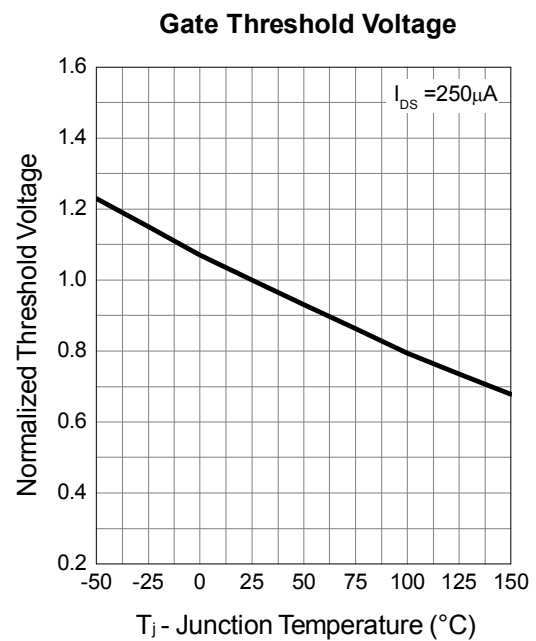
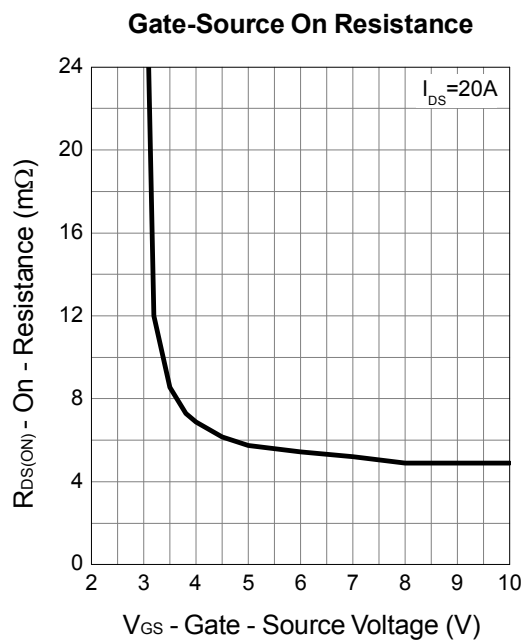
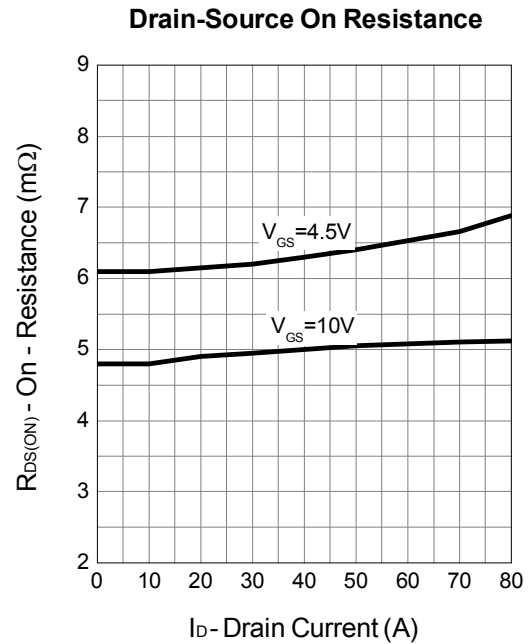
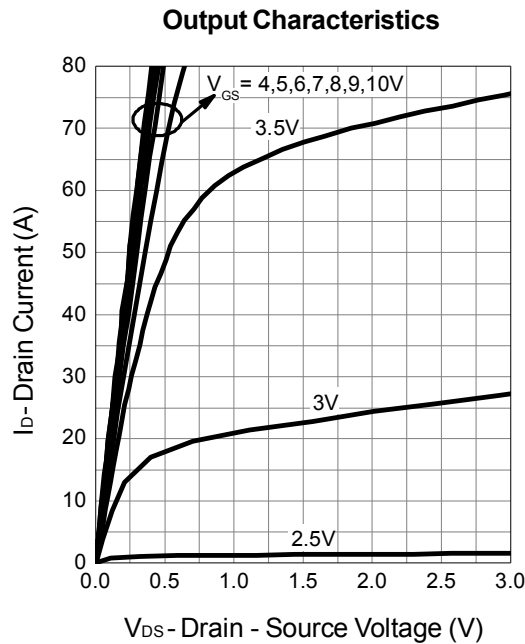
Note a : Pulse test ; pulse width ≤ 300 μs, duty cycle ≤ 2%.

Note b : Guaranteed by design, not subject to production testing.

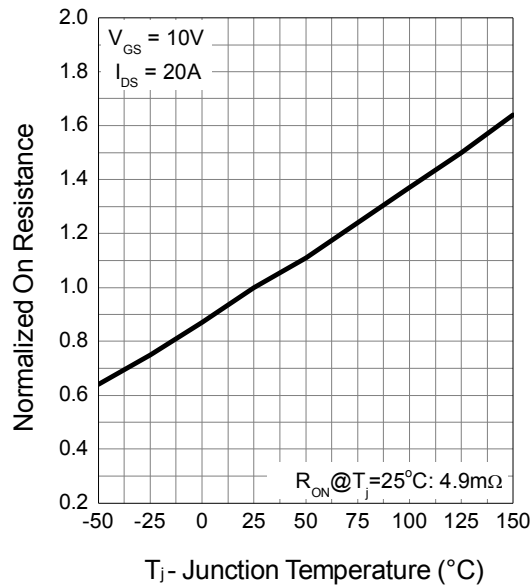
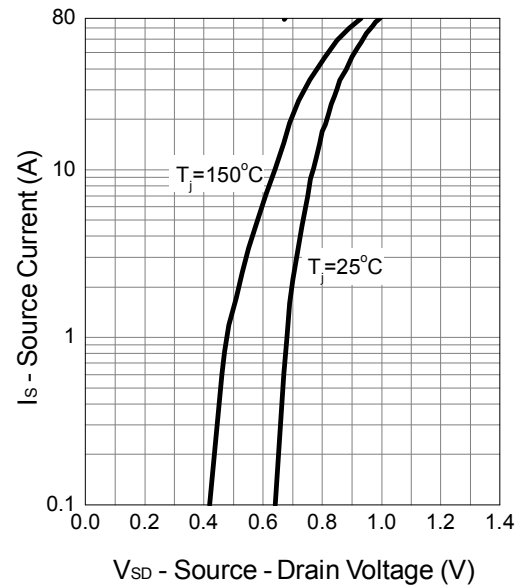
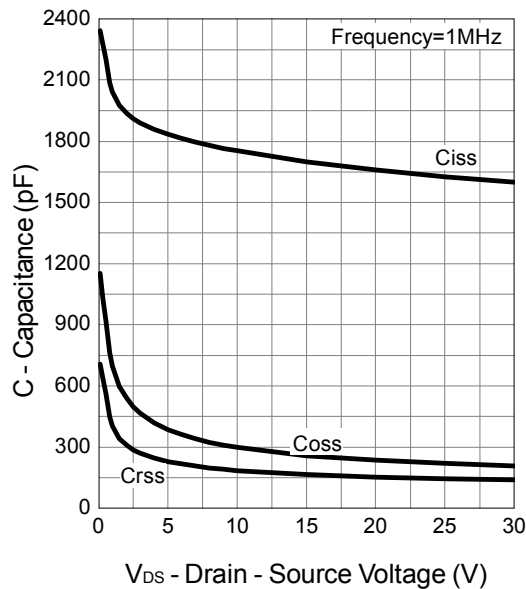
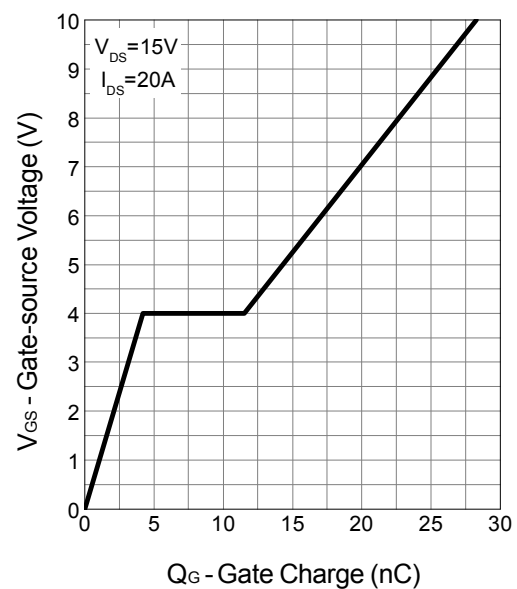
Typical Operating Characteristics



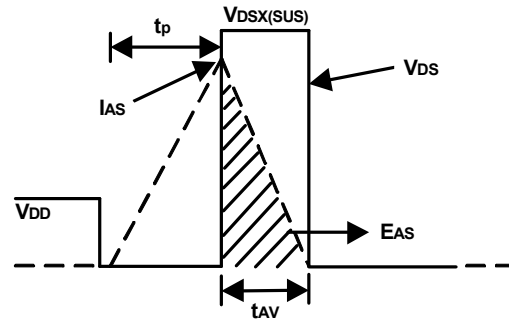
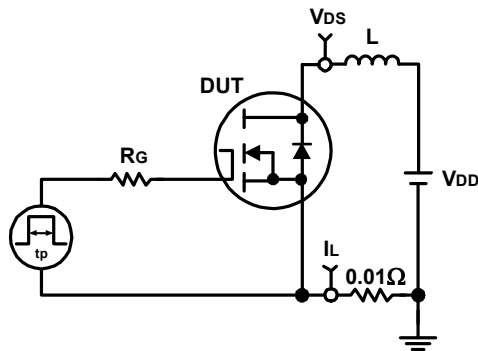
Typical Operating Characteristics (Cont.)



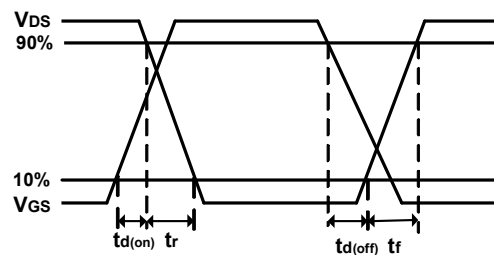
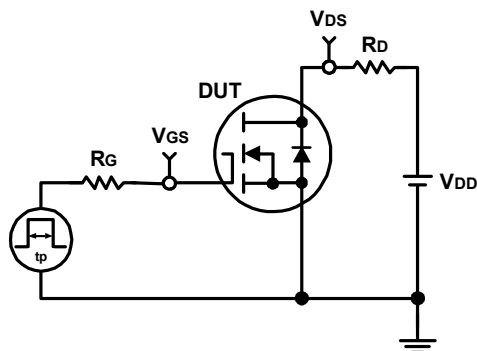
Typical Operating Characteristics (Cont.)

Drain-Source On Resistance

Source-Drain Diode Forward

Capacitance

Gate Charge


Avalanche Test Circuit and Waveforms

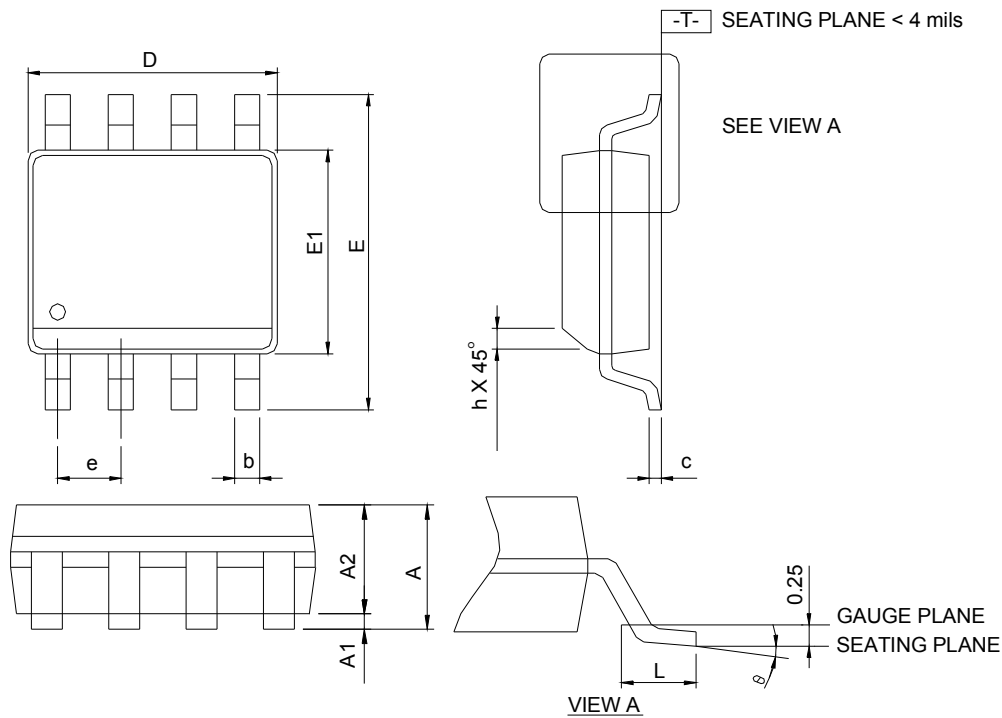


Switching Time Test Circuit and Waveforms



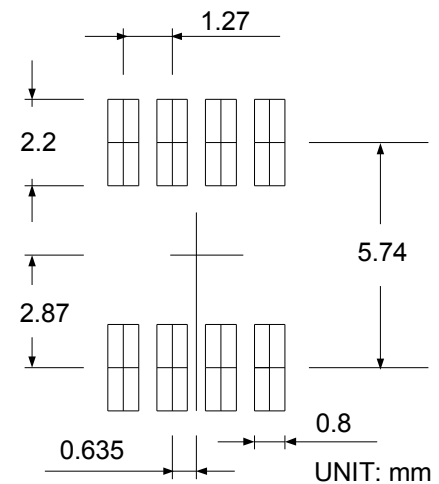
Package Information

SOP-8



DIMENSIONS	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.