

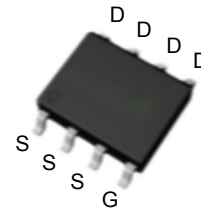
Features

- -30V/-13A,
 $R_{DS(ON)} = 11m\Omega (typ.) @ V_{GS} = -10V$
 $R_{DS(ON)} = 16m\Omega (typ.) @ V_{GS} = -4.5V$
- Reliable and Rugged
- 100% UIS + R_g Tested
- Lead Free and Green Devices Available
(RoHS Compliant)

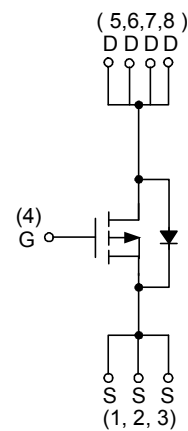
Applications

- Power Management in Notebook Computer, Portable Equipment and Battery Powered Systems.

Pin Description



Top View of SOP-8



P-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Symbol	Parameter		Rating	Unit
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		± 25	
I_D^a	Continuous Drain Current ($V_{GS} = -10\text{V}$)	$T_A = 25^\circ\text{C}$	-13	A
		$T_A = 70^\circ\text{C}$	-10.5	
I_{DM}^a	Pulsed Drain Current ($V_{GS} = -10\text{V}$)		-60	
I_S^a	Diode Continuous Forward Current		-4	
I_{AS}^b	Avalanche Current, Single pulse ($L = 0.3\text{mH}$)		-26	
E_{AS}^b	Avalanche Energy, Single pulse ($L = 0.3\text{mH}$)		101	mJ
T_J	Maximum Junction Temperature		150	$^\circ\text{C}$
T_{STG}	Storage Temperature Range		-55 to 150	
P_D^a	Maximum Power Dissipation	$T_A = 25^\circ\text{C}$	3.1	W
		$T_A = 70^\circ\text{C}$	2	
$R_{\theta JA}^{a,c}$	Thermal Resistance-Junction to Ambient	$t \leq 10\text{s}$	40	$^\circ\text{C/W}$
		Steady State	75	
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	Steady State	24	

Note a : Surface Mounted on 1in^2 pad area, $t \leq 10\text{sec}$.

Note b : UIS tested and pulse width limited by maximum junction temperature (initial temperature $T_J = 25^\circ\text{C}$).

Note c : Maximum under Steady State conditions is 75°C/W .

Electrical Characteristics (T_A = 25°C Unless Otherwise Noted)

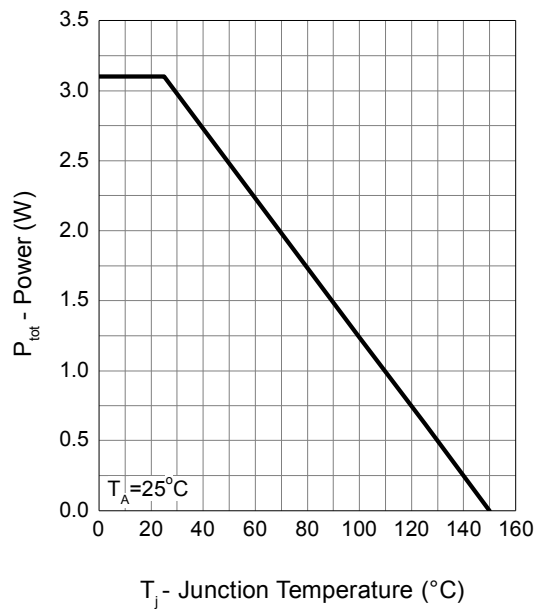
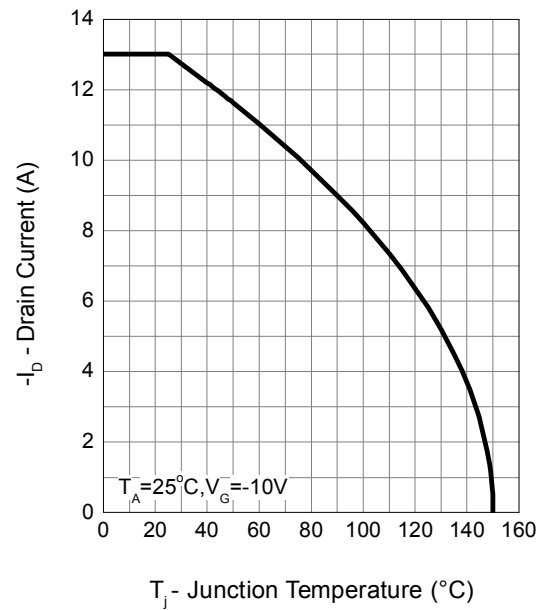
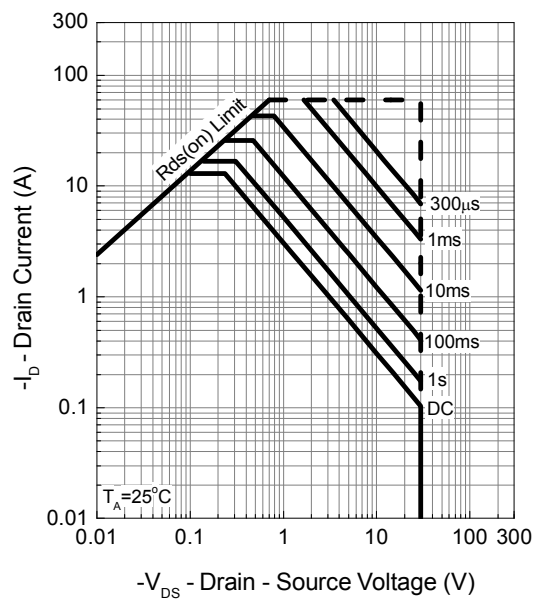
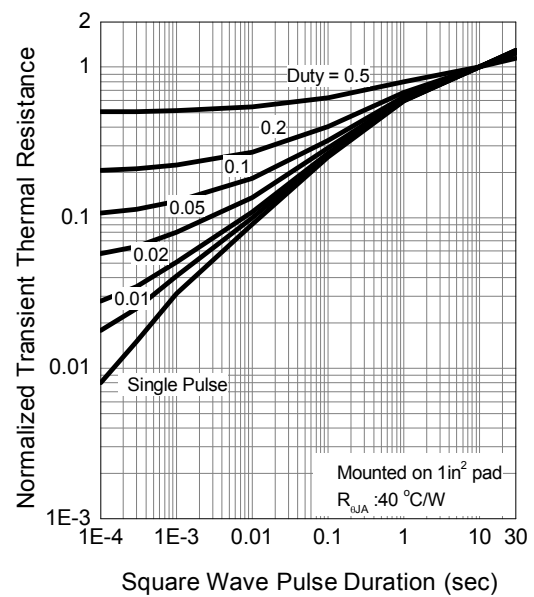
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =-250μA	-30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-24V, V _{GS} =0V	-	-	-1	μA
		T _J =85°C	-	-	-30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =-250μA	-1.5	-2	-2.5	V
I _{GSS}	Gate Leakage Current	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)} ^d	Drain-Source On-state Resistance	V _{GS} =-10V, I _{DS} =-13A	-	11	15	mΩ
		V _{GS} =-4.5V, I _{DS} =-5A	-	16	20	
Diode Characteristics						
V _{SD} ^d	Diode Forward Voltage	I _{SD} =-1A, V _{GS} =0V	-	-0.7	-1	V
t _{rr} ^e	Reverse Recovery Time	I _{SD} =-13A, di _{SD} /dt=100A/μs	-	22	-	ns
Q _{rr} ^e	Reverse Recovery Charge		-	15	-	nC
Dynamic Characteristics ^e						
R _g	Gate Resistance	V _{GS} =0V, V _{DS} =0V, F=1MHz	-	2	3.6	Ω
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-15V, Frequency=1.0MHz	-	1550	-	pF
C _{oss}	Output Capacitance		-	315	-	
C _{rss}	Reverse Transfer Capacitance		-	245	-	
t _{d(ON)}	Turn-on Delay Time	V _{DD} =-15V, R _L =15Ω, I _{DS} =-1A, V _{GEN} =-10V, R _G =6Ω	-	13	-	ns
t _r	Turn-on Rise Time		-	15	-	
t _{d(OFF)}	Turn-off Delay Time		-	50	-	
t _f	Turn-off Fall Time		-	29	-	
Gate Charge Characteristics ^e						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _{DS} =-13A	-	31	40	nC
Q _{gs}	Gate-Source Charge		-	4.3	-	
Q _{gd}	Gate-Drain Charge		-	10	-	

Note d : Pulse test ; pulse width≤300μs, duty cycle≤2%.

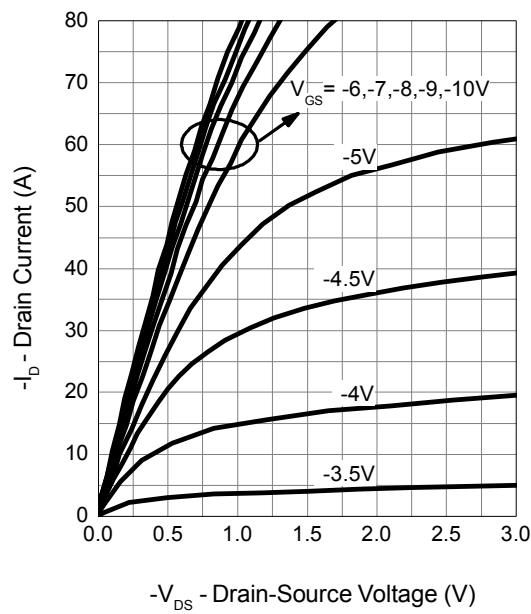
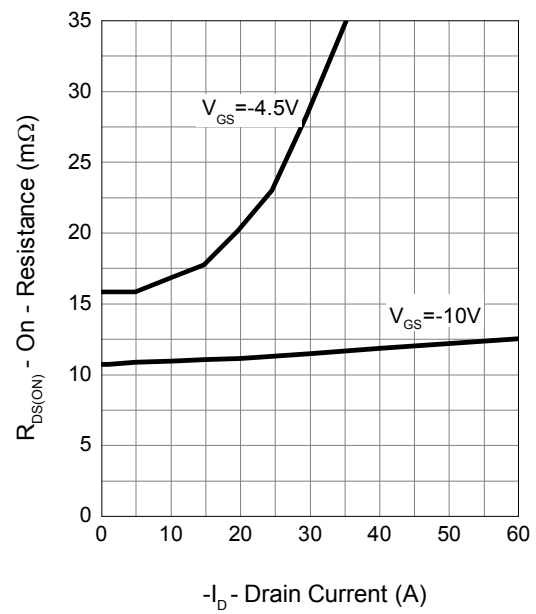
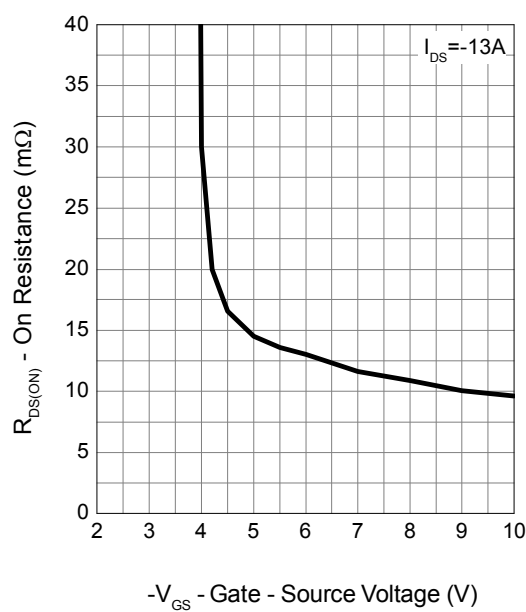
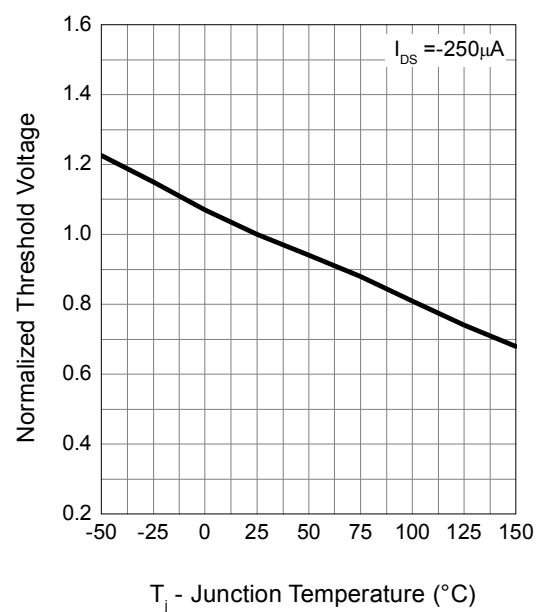
Note e : Guaranteed by design, not subject to production testing.

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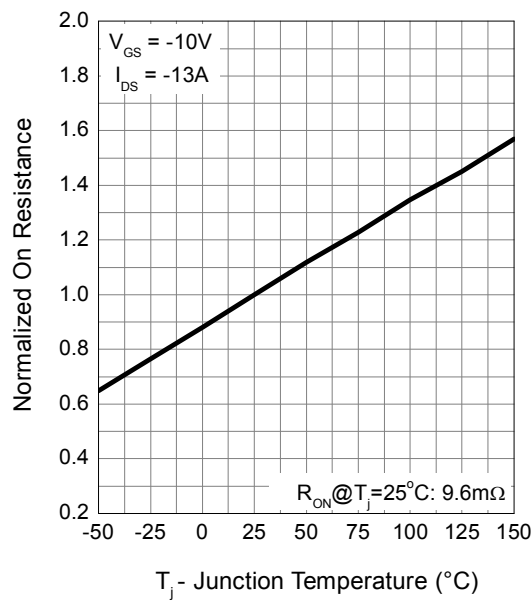
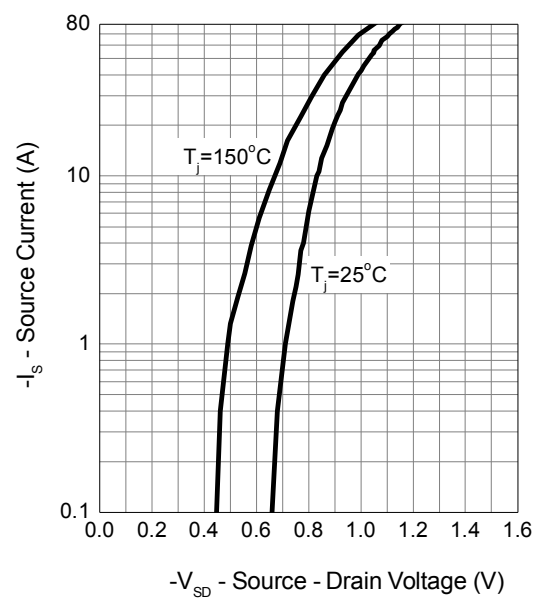
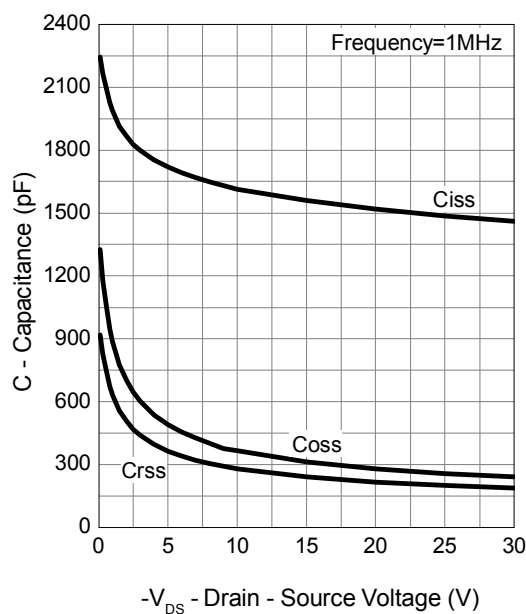
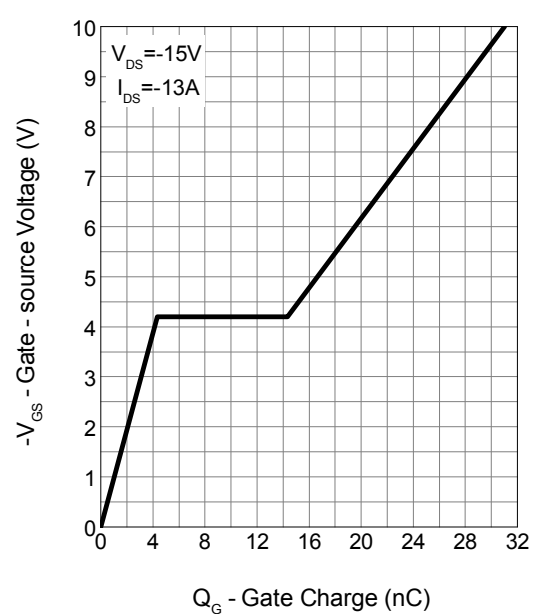
Typical Operating Characteristics

Power Dissipation

Drain Current

Safe Operation Area

Thermal Transient Impedance


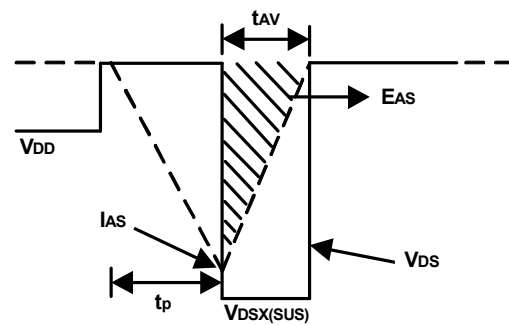
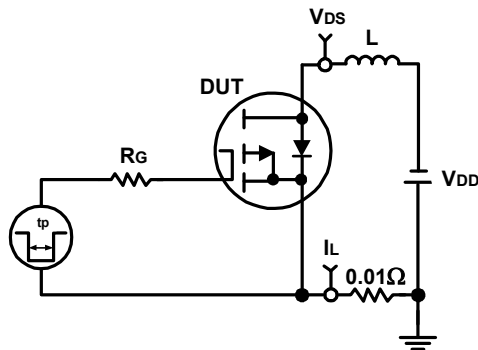
Typical Operating Characteristics (Cont.)

Output Characteristics

Drain-Source On Resistance

Gate-Source On Resistance

Gate Threshold Voltage


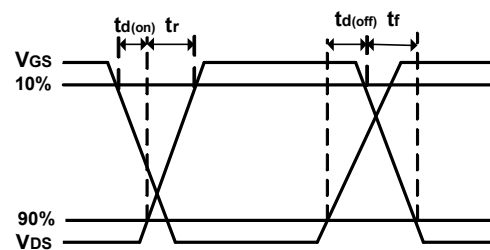
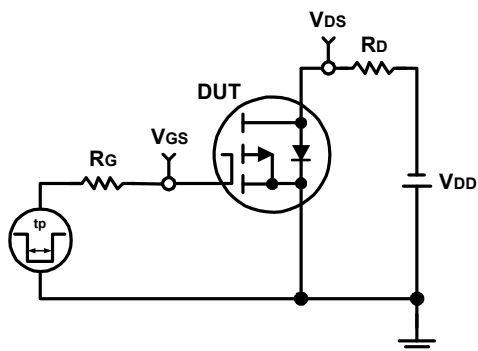
Typical Operating Characteristics (Cont.)

Drain-Source On Resistance

Source-Drain Diode Forward

Capacitance

Gate Charge


Avalanche Test Circuit and Waveforms

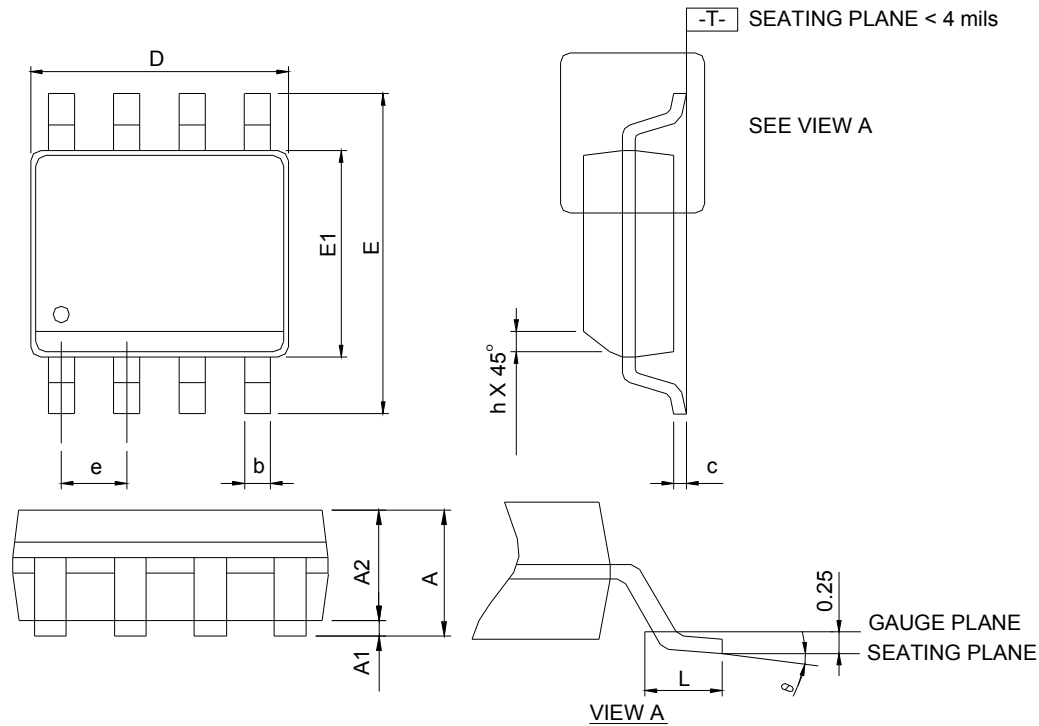


Switching Time Test Circuit and Waveforms



Package Information

SOP-8



SOP-8	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

