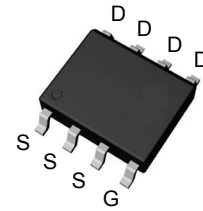


- 30V/13A
- $R_{DS(ON)} = 7.5m\Omega$ (typ) @ $V_{GS} = 10V$
 $R_{DS(ON)} = 11m\Omega$ (typ) @ $V_{GS} = 4.5V$
- 100% UIS & RG Tested
- Reliable and Rugged
- Lead Free and Green Devices Available
(RoHS Compliant)

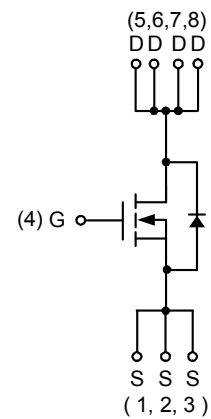
Applications

- Power Management for Industrial DC/DC Converters

Pin Description



Top View of SOP-8



N-Channel MOSFET

Absolute Maximum Ratings (T_A= 25°C unless otherwise noted)

Symbol	Parameter		Rating	Unit
Common Ratings				
V _{DSS}	Drain-Source Voltage		30	V
V _{GSS}	Gate-Source Voltage		±20	
I _D	Continuous Drain Current	T _j =150°C	13	A
I _{DM}	Pulsed Drain Current		39	
I _S	Diode Continuous Forward Current		13	A
T _{STG} , T _j	Storage Temperature Range		-55 to 150	°C
P _D	Power Dissipation	T _A =25°C	2.8	W
		T _A =70°C	1.8	
R _{θJA}	Thermal Resistance-Junction to Ambient		62.5	

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _{DS} =250μA	30	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =24V, V _{GS} =0V	-	-	1	μA
		T _J =85°C	-	-	30	
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250μA	1	-	2	V
I _{GSS}	Gate Leakage Current	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
R _{DS(ON)}	Drain-Source On-state Resistance	V _{GS} =10V, I _{DS} =13A	-	7.5	9.5	mΩ
		V _{GS} =4.5V, I _{DS} =10A	-	11	14	
Body Diode Characteristics						
V _{SD}	Diode Forward Voltage	I _{SD} =2A, V _{GS} =0V	-	0.7	1.3	V
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =25V, Frequency=1.0MHz	-	770	-	pF
C _{oss}	Output Capacitance		-	110	-	
C _{rss}	Reverse transfer capacitance		-	90	-	
t _{d(ON)}	Turn-on delay Time	V _{GS} =10V, V _{DS} =15V R _G =6Ω, I _D =1A, R _L =15Ω	-	5	-	nS
t _r	Turn-on rise Time		-	3.5	-	
t _{d(OFF)}	Turn-off delay Time		-	19	-	
t _f	Turn-off rise Time		-	3.5	-	
Gate Charge Characteristics						
Q _g	Total Gate Charge	V _{DS} =15V, V _{GS} =10V, I _{DS} =9A	-	11.6	-	nC
Q _{gs}	Gate-Source Charge		-	2.5	-	
Q _{gd}	Gate-Drain Charge		-	3.9	-	

Note: 1. Pulse test: pulse width≤300uS, duty cycle≤2%

2.Static parameters are based on package level with recommended wire bonding

TYPICAL CHARACTERISTICS (25 °C Unless Note)

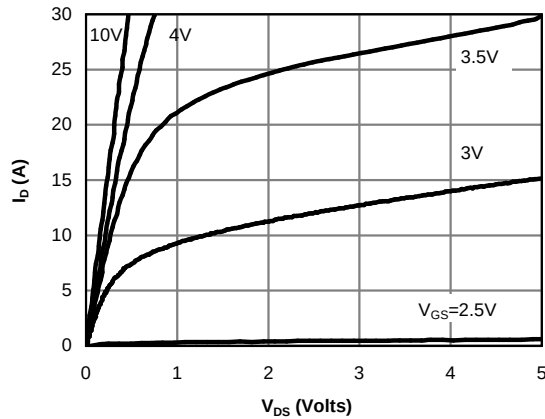


Fig 1: On-Region Characteristics (Note E)

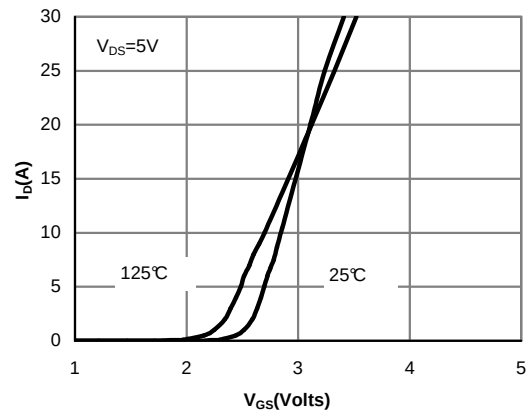


Figure 2: Transfer Characteristics (Note E)

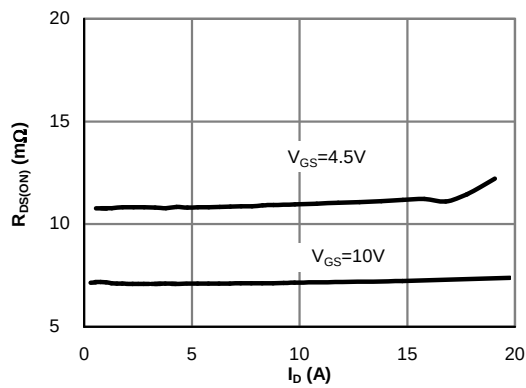


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

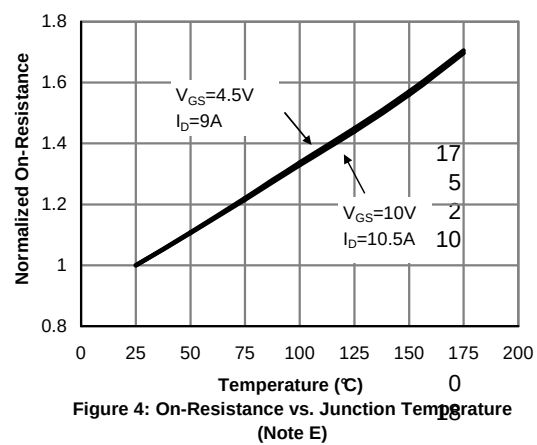


Figure 4: On-Resistance vs. Junction Temperature (Note E)

TYPICAL CHARACTERISTICS (continuous)

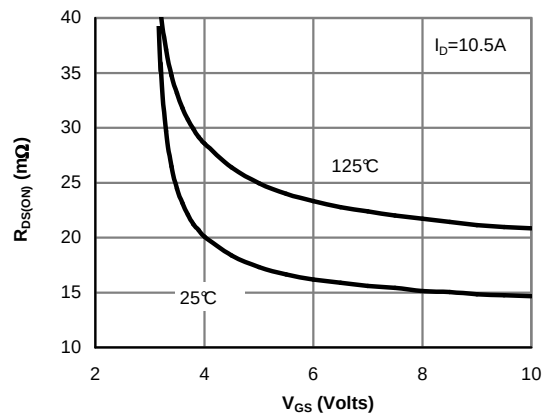


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

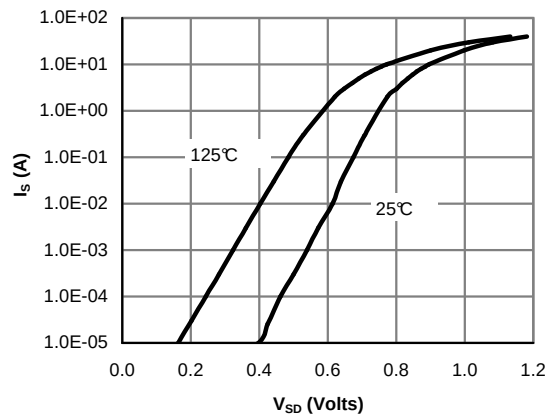


Figure 6: Body-Diode Characteristics (Note E)

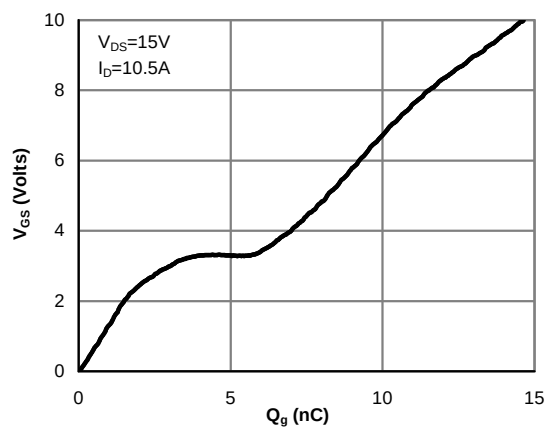


Figure 7: Gate-Charge Characteristics

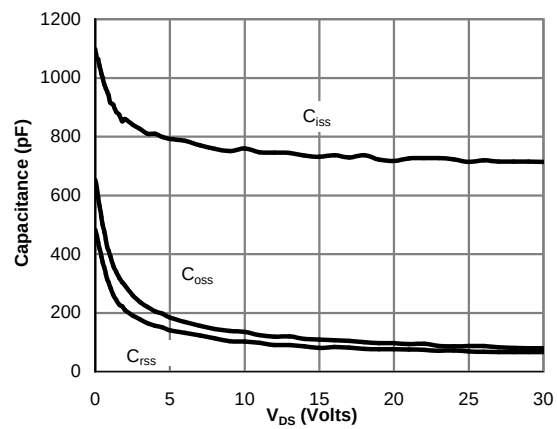


Figure 8: Capacitance Characteristics

TYPICAL CHARACTERISTICS (continuous)

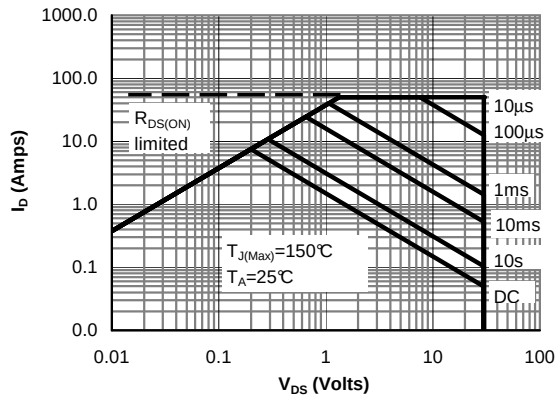


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

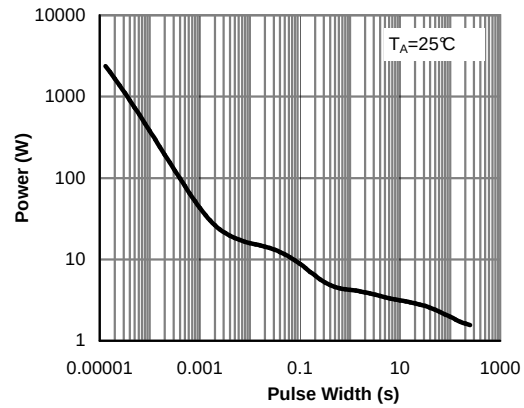


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

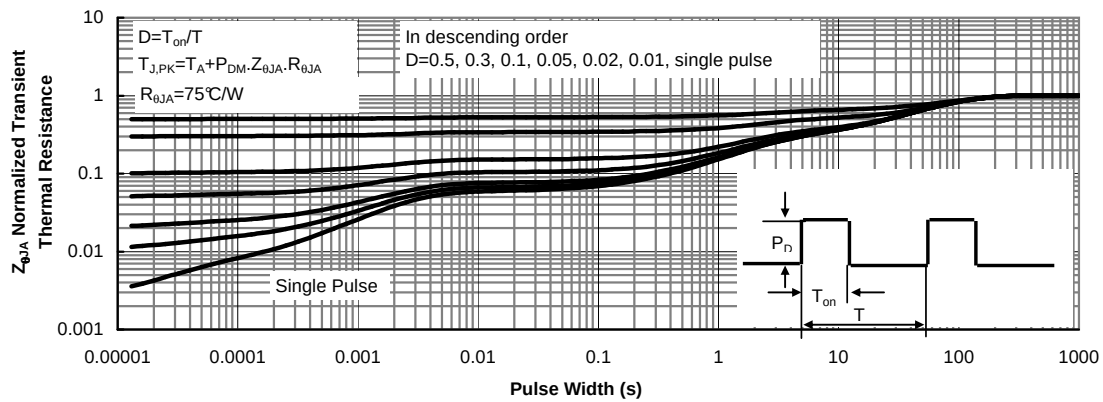
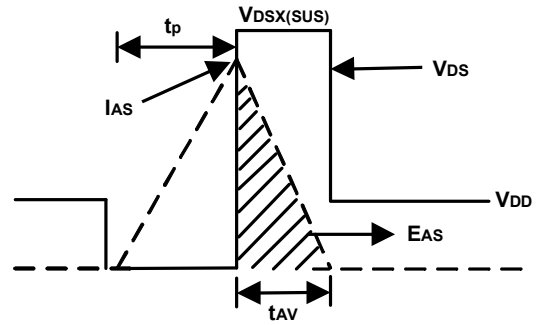
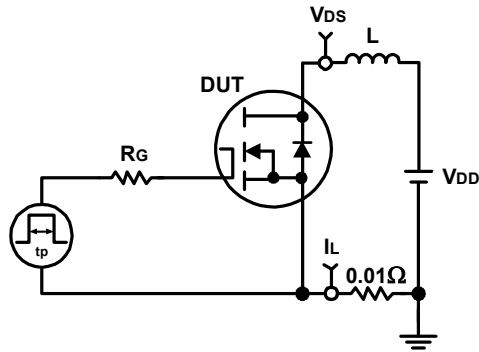
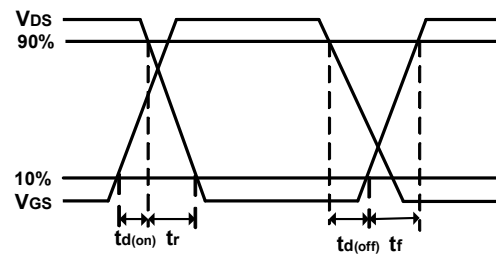
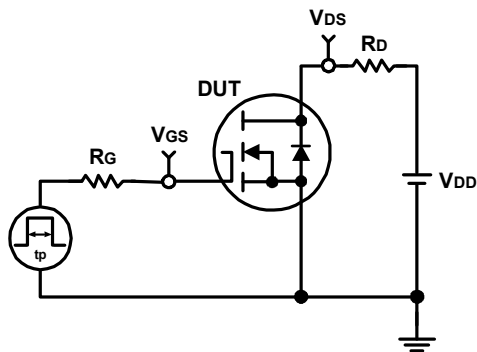


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

Avalanche Test Circuit and Waveforms

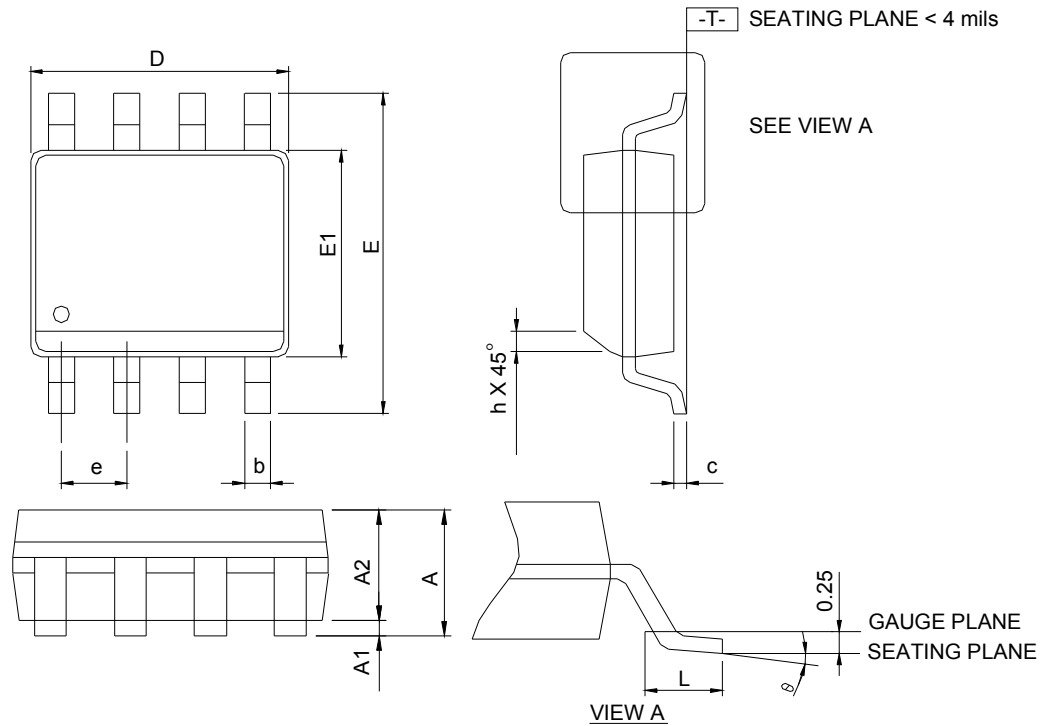


Switching Time Test Circuit and Waveforms



Package Information

SOP-8



SOP-8	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

RECOMMENDED LAND PATTERN

