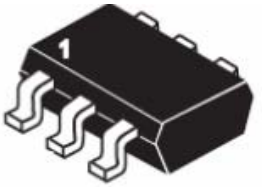
Dual P-Channl Enhancement Mode MOSFET

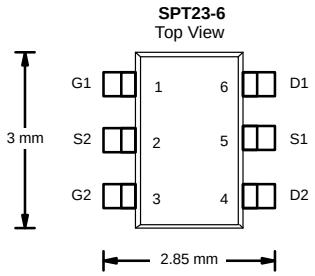
- -30V/-4A
- $R_{DS(ON)}$=45mΩ (typ) @VGS=10V
  $R_{DS(ON)}$=48mΩ (typ) @VGS=4.5V
  $R_{DS(ON)}$=65mΩ (typ) @VGS=2.5V
- 100% UIS & RG Tested
- Reliableand Rugged
- Lead Freeand Green Devices Available
  (RoHS Compliant)

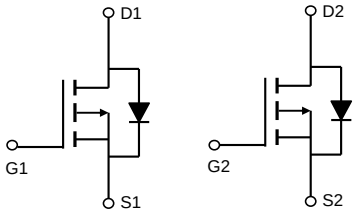
SOT23-6



Applic

- Power Management for Industrial
  Converters





Absolute Maximum Ratings (T = 25°C unless otherwise noted)

Symbol	Parameter		Rating	Unit
Common Ratings				
V_{DSS}	Drain-Source Voltage		-30	V
V_{GSS}	Gate-Source Voltage		±12	
I_D	Continuous Drain Current	T_A=25°C	-4	A
		T_A=70°C	-3.3	
I_{DM}	Pulsed Drain Current		-28	
T_{STG}, T_j	Storage Temperature Range		-55 to 150	°C
P_D	Power Dissipation	T_A=25°C	2	W
		T_A=70°C	1.3	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	t ≤ 10s	47.5	
		Steady-State	74	
$R_{\theta JL}$	Thermal Resistance-Junction to Lead		37	°C/W

Electrical Characteristics (Tj = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=-250A	-45	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} =-24V, V_{GS}=0V	-	-	-1	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} =V_{GS}, I_{DS}=-250uA	-1.5	-	-0.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=-2A	15	-	65	mΩ
		V_{GS}=4.5V, I_{DS}=-2A	20	-	68	
		V_{GS}=2.5V, I_{DS}=-1A	40	-	90	
Body Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD}=-1A, V_{GS}=0V	-1	-	-0.35	V
t_{rr}	Reverse Recovery Time	V_R=-22.5V I_{DS}=-2A, dI_{SD}/dt=100A/μs	-	11	13.5	ns
Qrr	Reverse Recovery Charge		-	3.5	-	nC
Dynamic Characteristics						
R_G	Gate Resistance	F=1MHz, V_{GS}=0V V_{DS}=0V	4	7.8	12	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS} =-22.5V, Frequency=1.0MHz	-	645	-	pF
C_{oss}	Output Capacitance		-	80	-	
C_{rss}	Reverse transfer capacitance		-	55	-	
$t_{d(ON)}$	Turn-on delay Time	V_{GS}=-10V ,VDS=-22.5V R_G=3Ω, R_L=3Ω	-	6.5	-	nS
t_r	Turn-on rise Time		-	3.5	-	
$t_{d(OFF)}$	Turn-off delay Time		-	41	-	
t_f	Turn-off rise Time		-	9	-	
Gate Charge Characteristics						
Q_g	Total Gate Charge (10V)	V_{DS} =-22.5V, V_{GS}=-10V, I_{DS}=-2A	-	14	-	nC
Q_g	Total Gate Charge (4.5V)			7		
Q_{gs}	Gate-Source Charge		-	1.5	-	
Q_{gd}	Gate-Drain Charge		-	2.5	-	

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

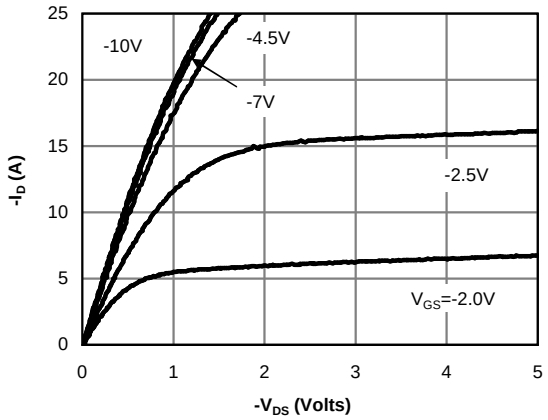


Fig 1: On-Region Characteristics (Note E)

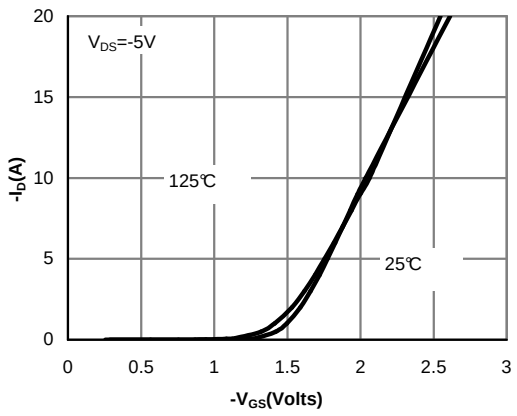


Figure 2: Transfer Characteristics (Note E)

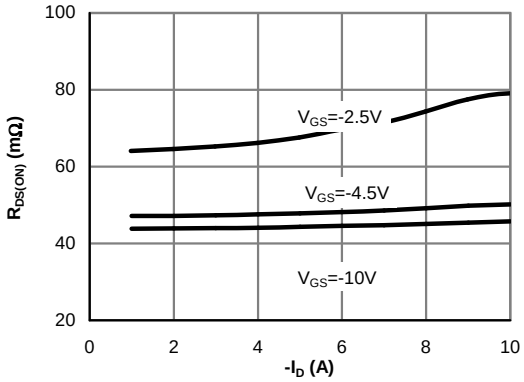


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

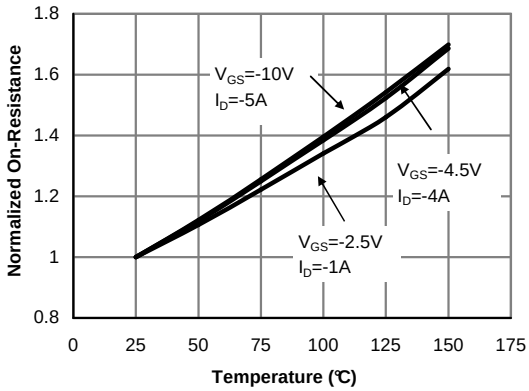


Figure 4: On-Resistance vs. Junction Temperature (Note E)

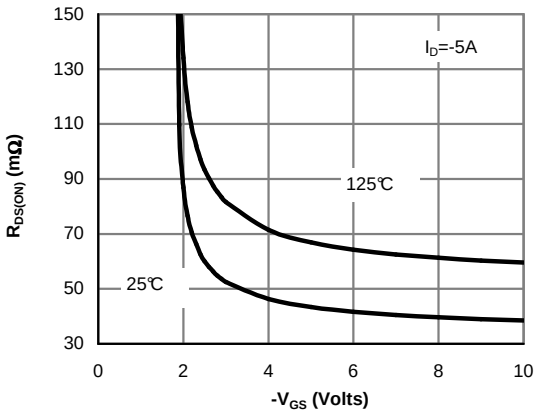


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

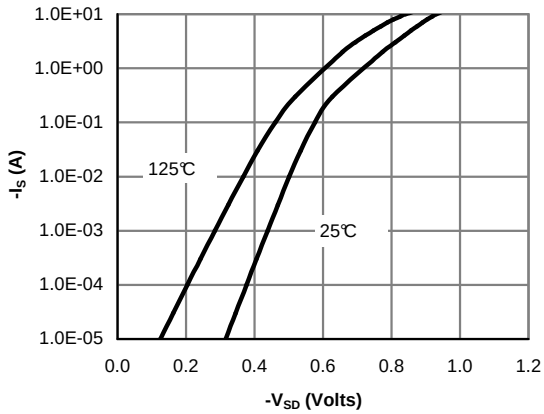


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

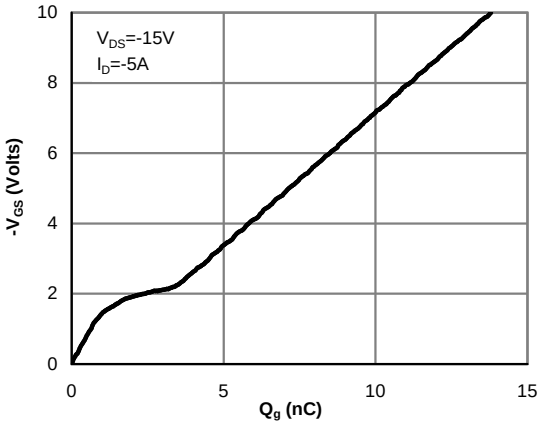


Figure 7: Gate-Charge Characteristics

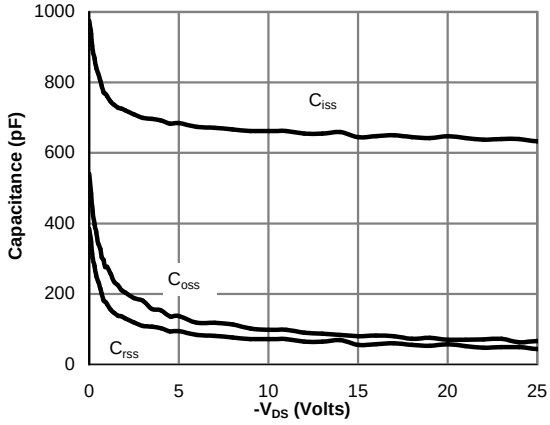


Figure 8: Capacitance Characteristics

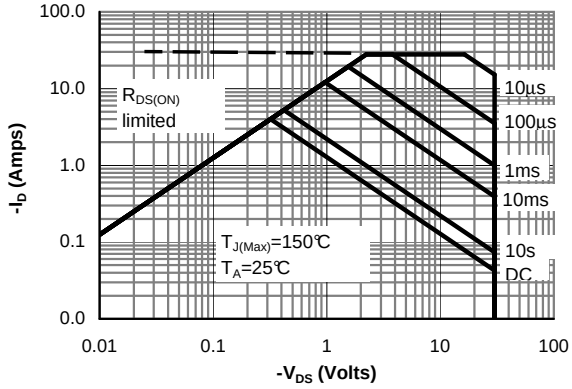


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

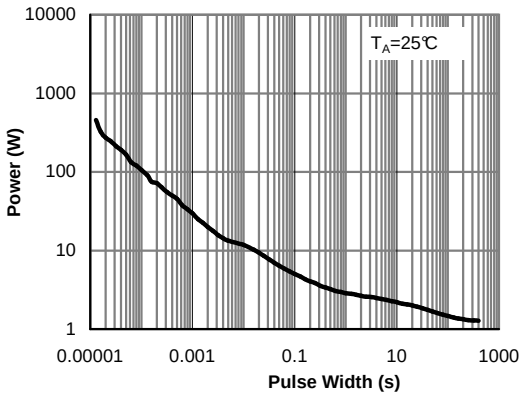


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

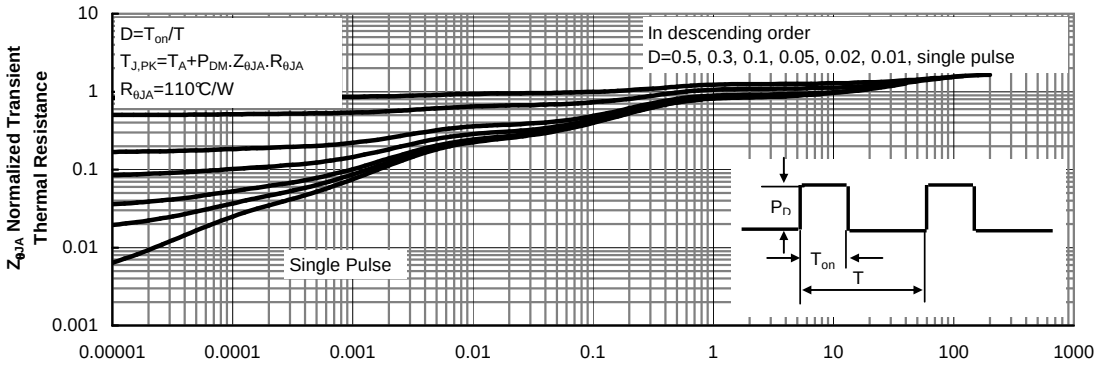
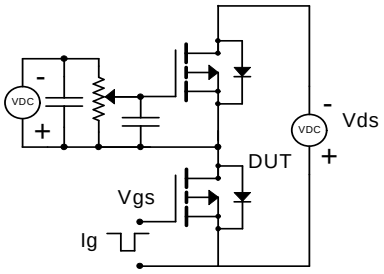
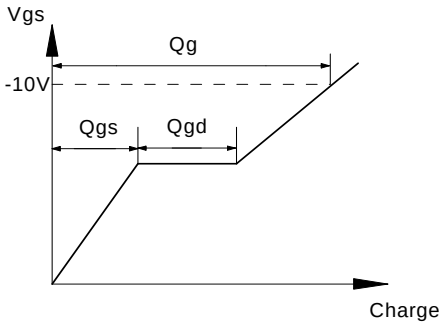


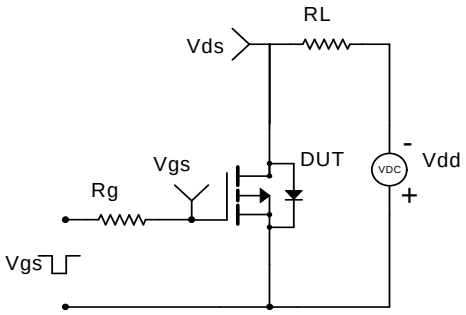
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

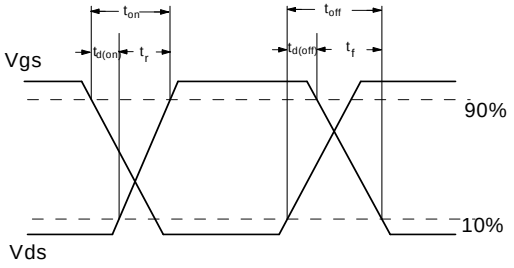
Gate Charge Test Circuit & Waveform



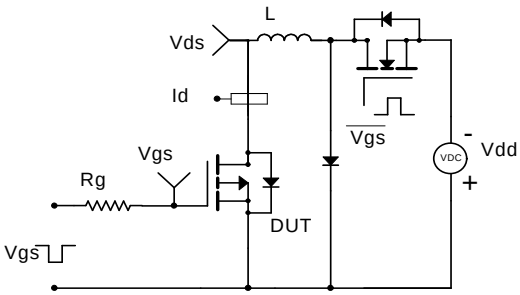


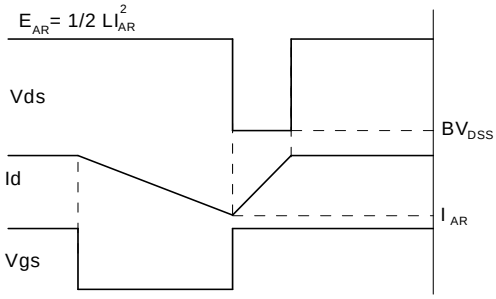
Resistive Switching Test Circuit & Waveforms



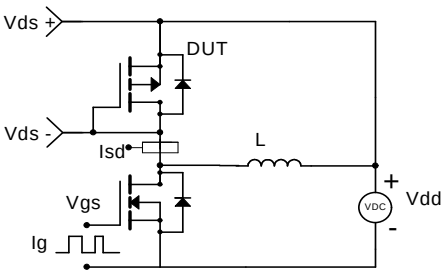


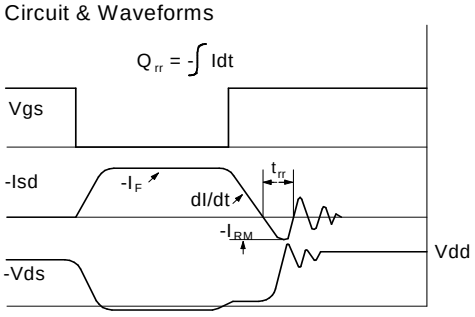
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



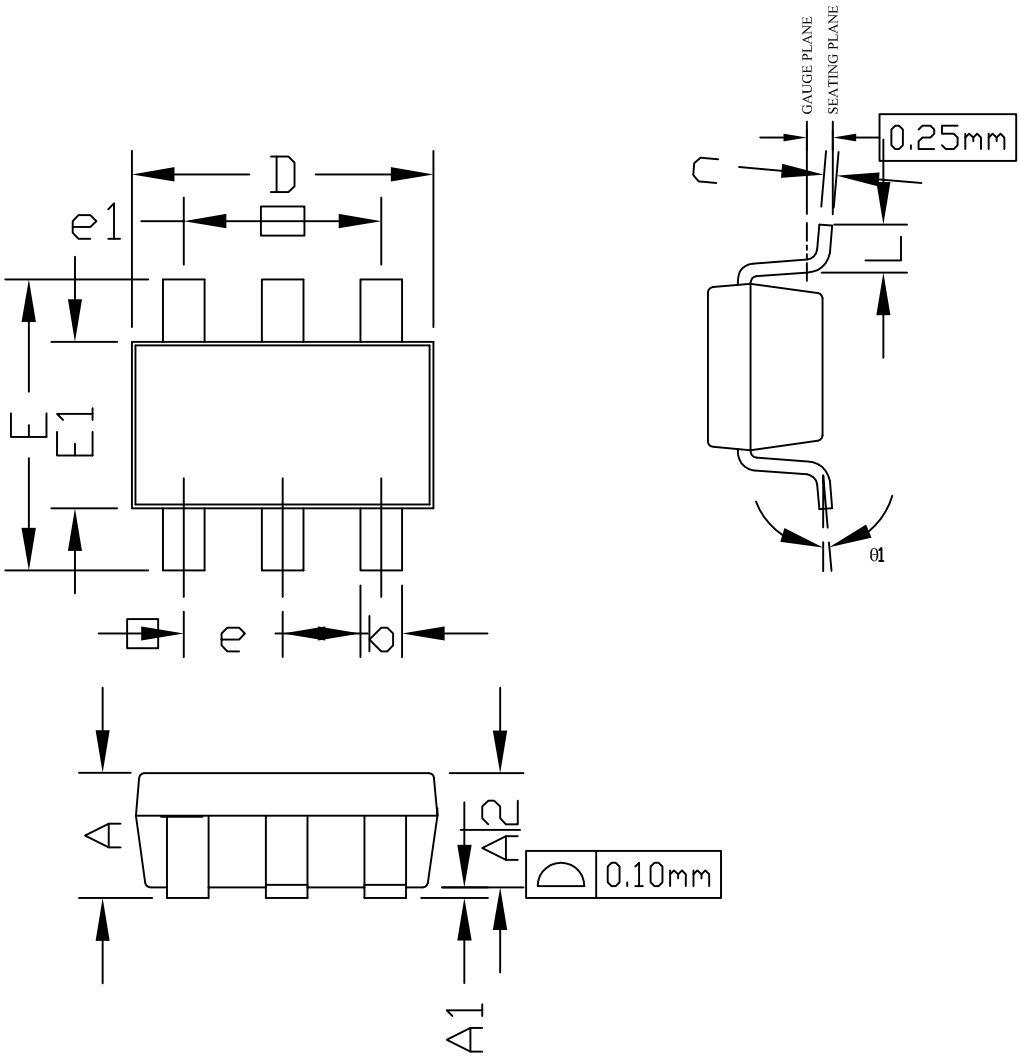


Diode Recovery Test Circuit & Waveforms

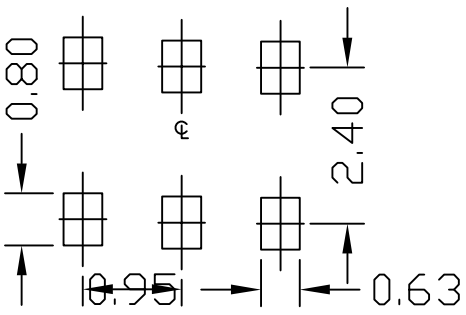




SOT23-6 PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	——	1.25	0.031	——	0.049
A1	0.00	——	0.15	0.000	——	0.006
A2	0.70	1.10	1.20	0.028	0.043	0.047
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.08	0.13	0.20	0.003	0.005	0.008
D	2.70	2.90	3.10	0.106	0.114	0.122
E	2.50	2.80	3.10	0.098	0.110	0.122
E1	1.50	1.60	1.70	0.059	0.063	0.067
e	0.95 BSC.			0.037BSC.		
e1	1.90 BSC.			0.075 BSC.		
L	0.30	——	0.60	0.012	——	0.024
θ1	0°	——	8°	0°	——	8°

UNIT: mm

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 5 MILS EACH.
2. DIMENSION "L" IS MEASURED IN GAUGE PLANE.
3. TOLERANCE ±0.100 mm(4 mil) UNLESS OTHERWISE SPECIFIED.
4. FOLLOWED FROM JEDEC MO-178C & MO-193C.
5. CONTROLLING DIMENSIONS IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.