

N-Channl Enhancement Mode MOSFET

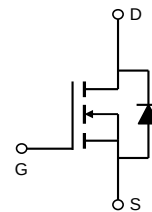
- 20V/4.2A
- $R_{DS(ON)}=35m\Omega$ (typ) @VGS=4.5V
 $R_{DS(ON)}=44m\Omega$ (typ) @VGS=2.5V
- 100% UIS & RG Tested
- Reliable and Rugged
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Power Management for Industrial DC/DC Converters

Pin Description

Top View of SOT-523



N-Channel MOSFET

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		Rating	Unit
Common Ratings				
V _{DSS}	Drain-Source Voltage		20	V
V _{GSS}	Gate-Source Voltage		±12	
ID	Continuous Drain Current	T _A =25°C	4.2	A
		T _A =70°C	3.3	
I _{DM}	Pulsed Drain Current ^C		18	
I _S	Diode Continuous Forward Current	T _c =25°C	-2	A
T _{STG} , T _J	Storage Temperature Range		-55 to 150	°C
PD	Power Dissipation ^B	T _A =25°C	1.25	W
		T _A =70°C	0.8	
R _{θJL}	Thermal Resistance-Junction to Lead		80	°C/W
R _{θJA}	Thermal Resistance-Junction to Ambient ^{A D}	t≤10S	90	°C/W
		Steady-State	125	

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$, $V_{GS}=0\text{V}$	20			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=20\text{V}$, $V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			1 5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}$, $V_{GS}=\pm 12\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$, $I_D=250\mu\text{A}$	0.5	0.8	1.1	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=4.5\text{V}$, $I_D=4.2\text{A}$		35	40	m Ω
		$T_J=125^\circ\text{C}$		40	43.6	
		$V_{GS}=2.5\text{V}$, $I_D=5\text{A}$		44	55	m Ω
		$V_{GS}=1.8\text{V}$, $I_D=5\text{A}$		55	67	m Ω
g_{FS}	Forward Transconductance	$V_{DS}=5\text{V}$, $I_D=6.5\text{A}$		50		S
V_{SD}	Diode Forward Voltage	$I_S=1\text{A}$, $V_{GS}=0\text{V}$		0.6	1	V
I_S	Maximum Body-Diode Continuous Current				2	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}$, $V_{DS}=10\text{V}$, $f=1\text{MHz}$		660		pF
C_{oss}	Output Capacitance			100		pF
C_{rss}	Reverse Transfer Capacitance			80		pF
R_g	Gate resistance	$f=1\text{MHz}$	2	4	6	Ω
SWITCHING PARAMETERS						
$Q_g(4.5\text{V})$	Total Gate Charge	$V_{GS}=4.5\text{V}$, $V_{DS}=10\text{V}$, $I_D=6.5\text{A}$		7	14	nC
Q_{gs}	Gate Source Charge			1		nC
Q_{gd}	Gate Drain Charge			2		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=4.5\text{V}$, $V_{DS}=10\text{V}$, $R_L=1.54\Omega$, $R_{GEN}=3\Omega$		7		ns
t_r	Turn-On Rise Time			10		ns
$t_{D(off)}$	Turn-Off DelayTime			32		ns
t_f	Turn-Off Fall Time			11		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=6.5\text{A}$, $di/dt=500\text{A}/\mu\text{s}$		8		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=6.5\text{A}$, $di/dt=500\text{A}/\mu\text{s}$		6		nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}=150^\circ\text{C}$, using $\leq 10\text{s}$ junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$. Ratings are based on low frequency and duty cycles to keep initial $T_J=25^\circ\text{C}$.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using $<300\mu\text{s}$ pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ\text{C}$. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

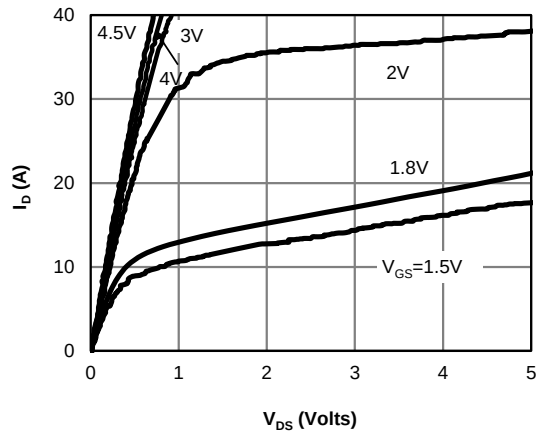


Figure 1: On-Region Characteristics (Note E)

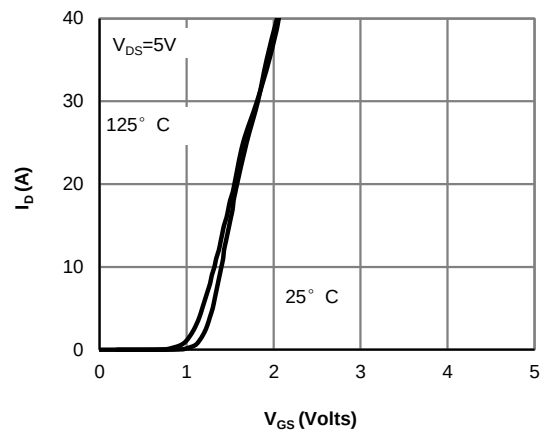


Figure 2: Transfer Characteristics (Note E)

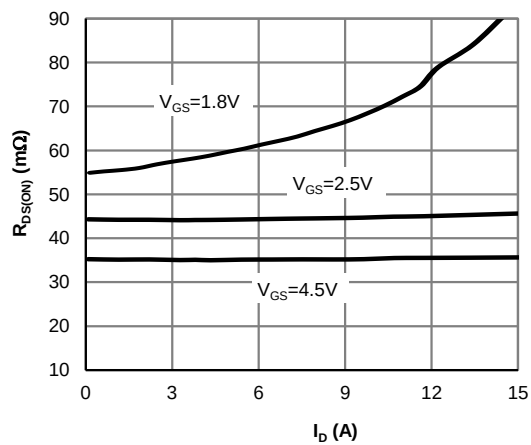


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

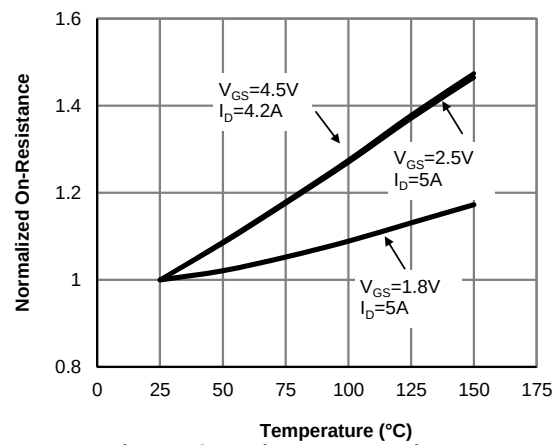
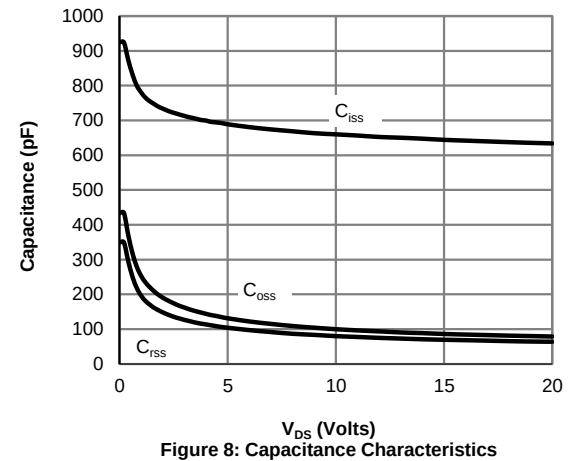
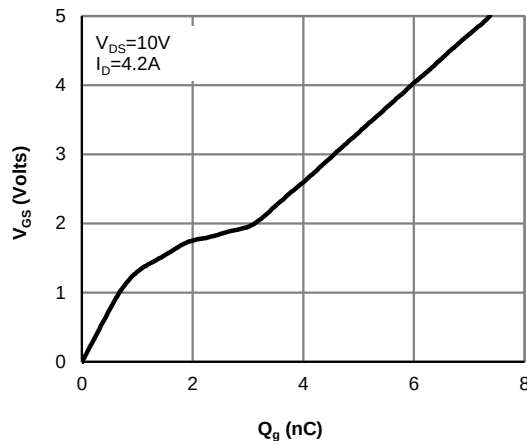
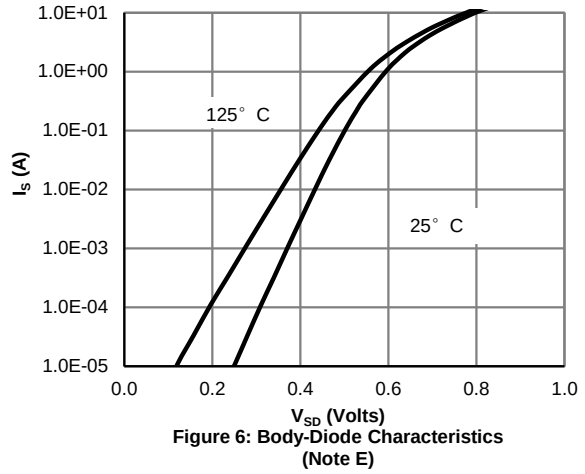
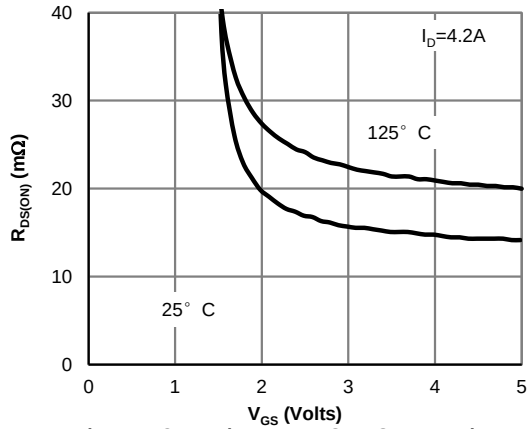


Figure 4: On-Resistance vs. Junction Temperature (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS



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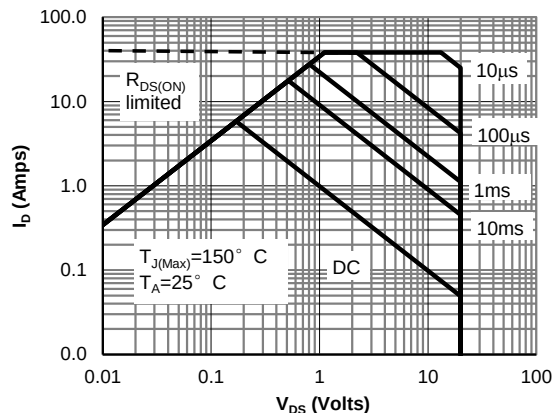


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

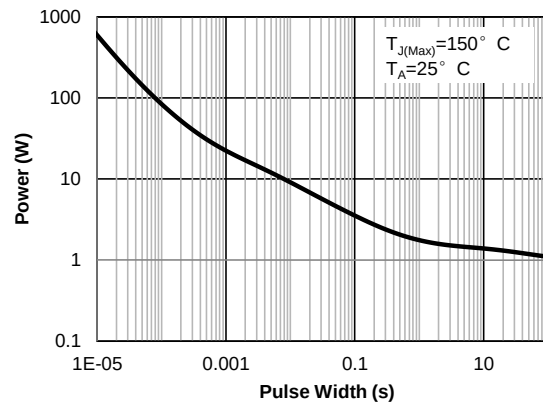


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

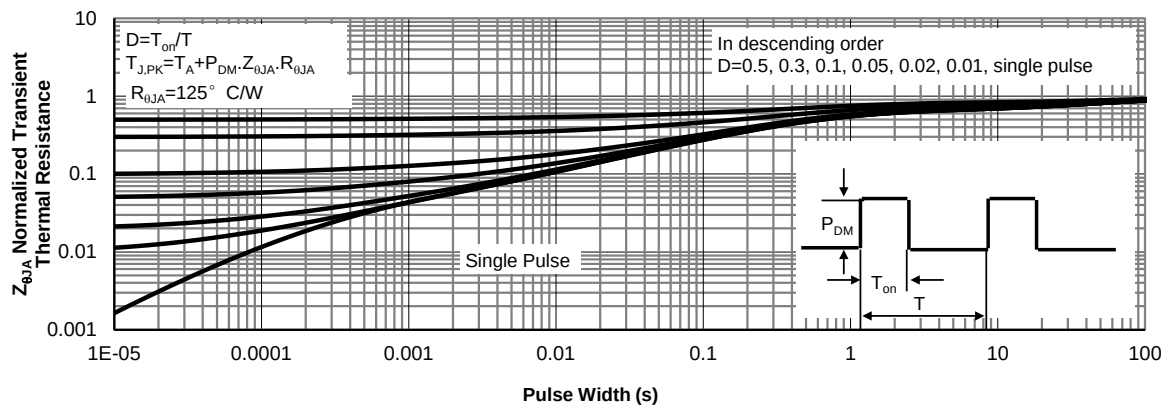
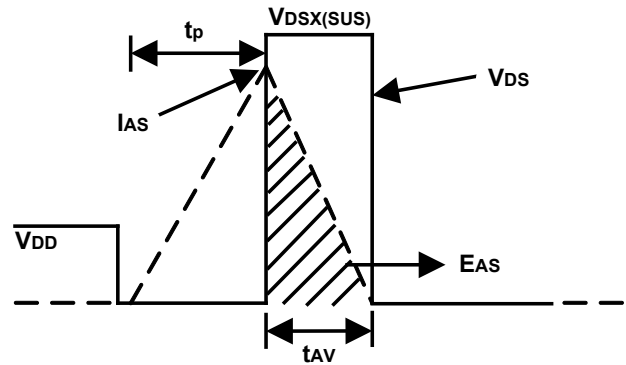
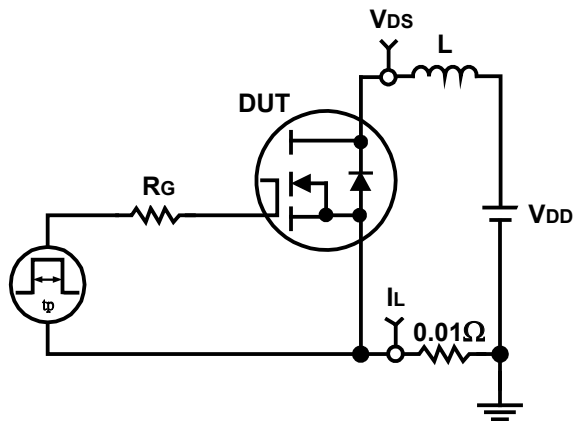
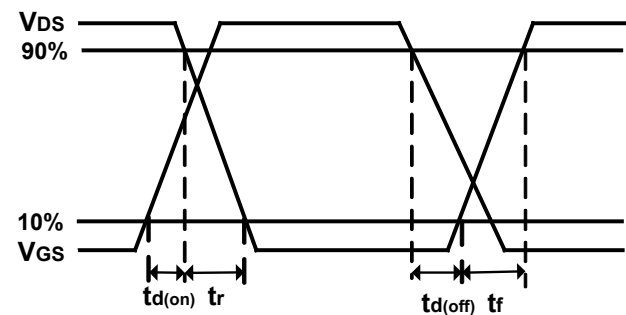
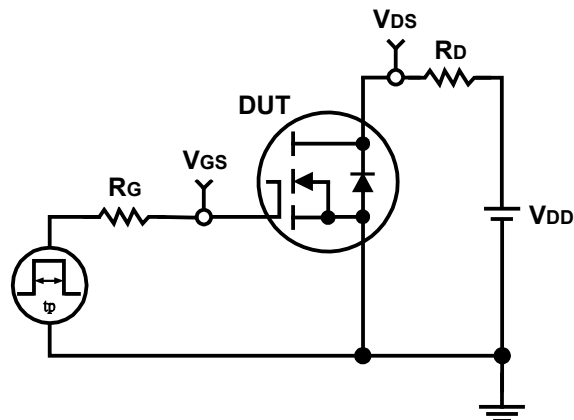


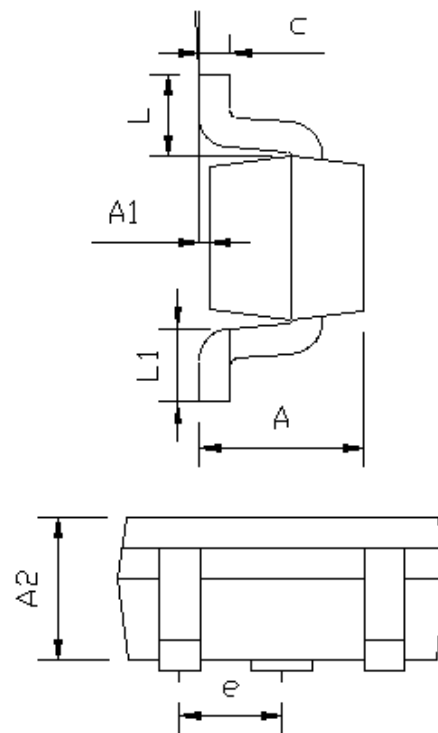
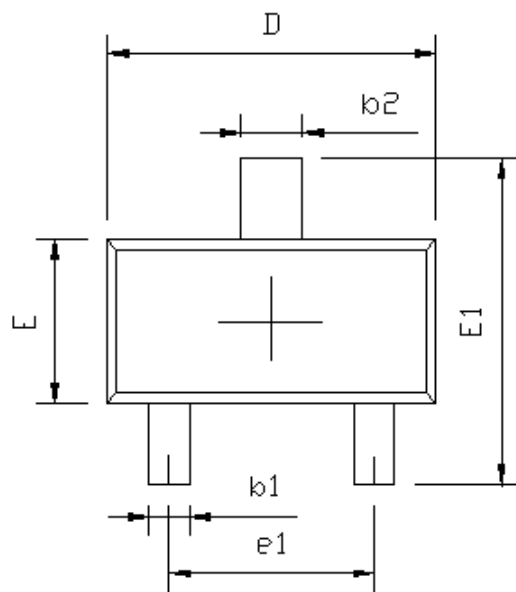
Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Avalanche Test Circuit and Waveforms



Switching Time Test Circuit and Waveforms





RECOMMENDED LAND PATTERN

