

Features

- Uses advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)

Application

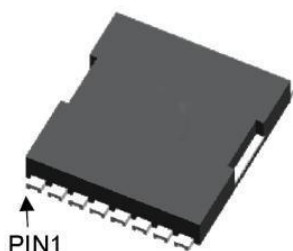
- Motor control and drive
- Battery management
- DC/DC

Product Summary

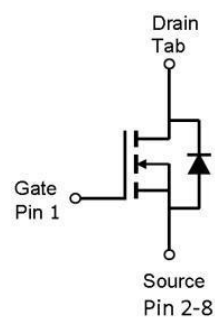
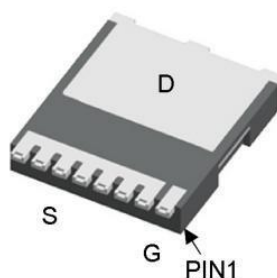
Package	TOLL
V_{DS}	150V
$R_{DS(on)}@V_{GS}=10V$	2.6mΩ
I_D	235A

Package Marking

TOLL Top View



TOLL Bottom View



Type	Package	Marking	Reel Size	Tape Width	Packing	Qty
LR030N15SW10	TOLL	LR030N15SW10	330*28.5mm	24mm	Reel&Tape	2000

Maximum Ratings (TC=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	150	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous drain current $T_c=25^\circ\text{C}$ (Silicon limit) $T_c=100^\circ\text{C}$ (Silicon limit)	I_D	235 143	A
Pulsed Drain Current	I_{DM}	940	A
Maximum Power Dissipation	P_d	367	W
Single pulse avalanche energy	E_{AS}	2116	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	°C

Thermal Characteristic

Thermal Resistance,Junction-to-Case	R_{thJC}	0.34	°C/W
Thermal Resistance,Junction-to-Ambient	R_{thJA}	62	

Electrical Characteristics (T_c=25°C unless otherwise noted)

Parameter	Symbol	Condition	min	typ	max	Unit
-----------	--------	-----------	-----	-----	-----	------

Static Characteristic

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	150	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	3.0	4.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=150V, V_{GS}=0V$	-	-	1	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$I_D=100A, V_{GS}=10V$	-	2.6	3.0	mΩ
Transconductance	g_{fs}	$V_{DS}=5V, I_D=100A$	-	261	-	S

Dynamic Characteristic

Input Capacitance	C_{iss}	$V_{DS}=75V, V_{GS}=0V,$ $f=1MHz$	-	11354	-	pF
Output Capacitance	C_{oss}		-	876	-	
Reverse Transfer Capacitance	C_{rss}		-	70	-	
Gate resistance	R_g	$f=1MHz$	-	1.9	-	Ω
Gate Total Charge	Q_G	$V_{DS}=75V, I_D=100A,$ $V_{GS}=10V$	-	178	-	nC
Gate-Source charge	Q_{gs}		-	73	-	
Gate-Drain charge	Q_{gd}		-	40	-	
Turn-on delay time	$t_{d(on)}$	$V_{GS}=10V, V_{DS}=75V,$ $R_G=2.7\Omega$	-	42	-	ns
Rise time	t_r		-	86	-	
Turn-off delay time	$t_{d(off)}$		-	99	-	
Fall time	t_f		-	43	-	

Body Diode Characteristic

Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=100A$	-	-	1.4	v
Reverse Recovery Time	t_{rr}	$I_F = 100A$ $di/dt = 100A/\mu s$	-	114	-	ns
Reverse Recovery Charge	Q_{rr}		-	464	-	nC

Typical Performance Characteristics

Fig 1: Output Characteristics

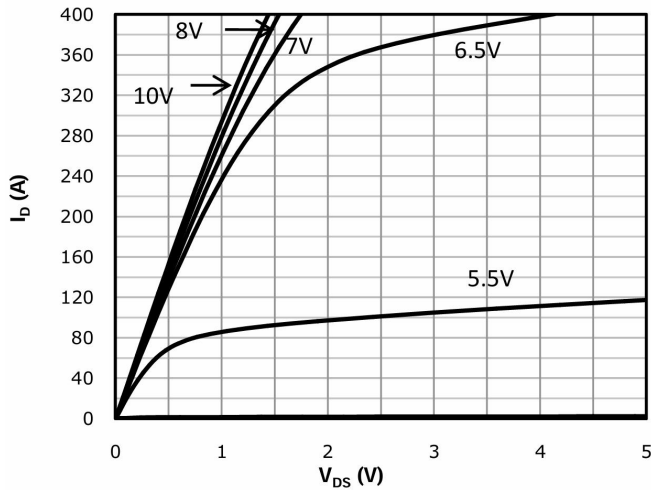


Fig 2: Transfer Characteristics

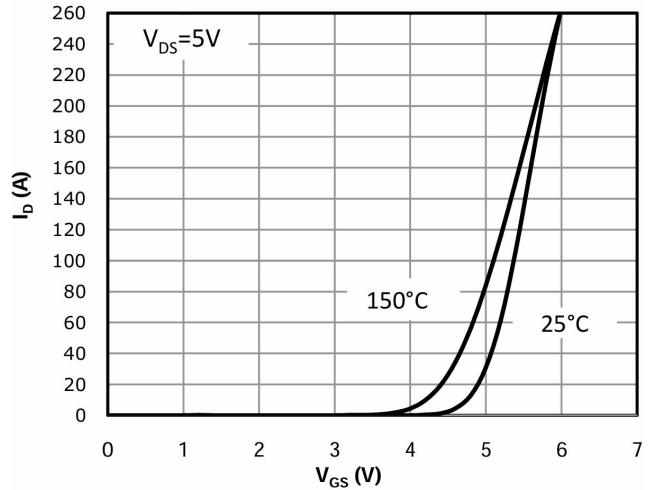


Fig 3: $R_{DS(on)}$ vs Drain Current and Gate Voltage

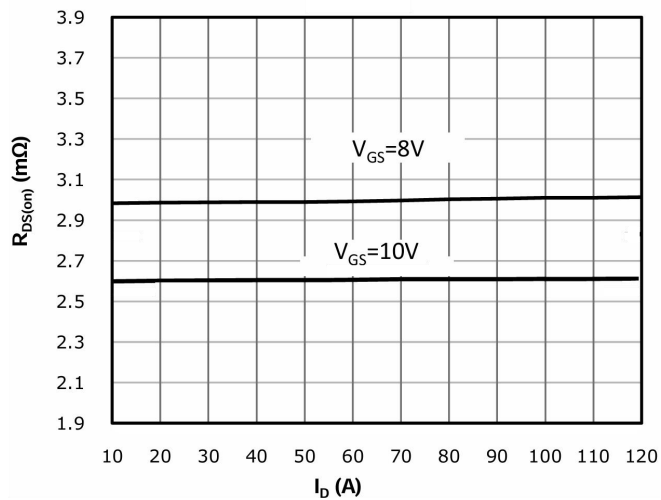


Fig 4: $R_{DS(on)}$ vs Gate Voltage

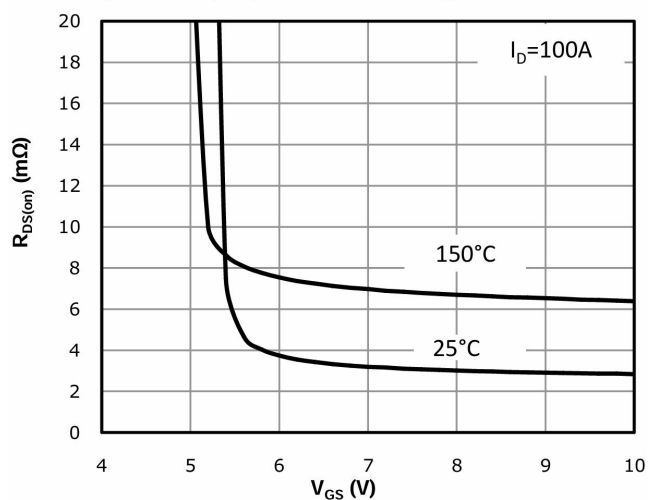


Fig 5: $R_{DS(on)}$ vs. Temperature

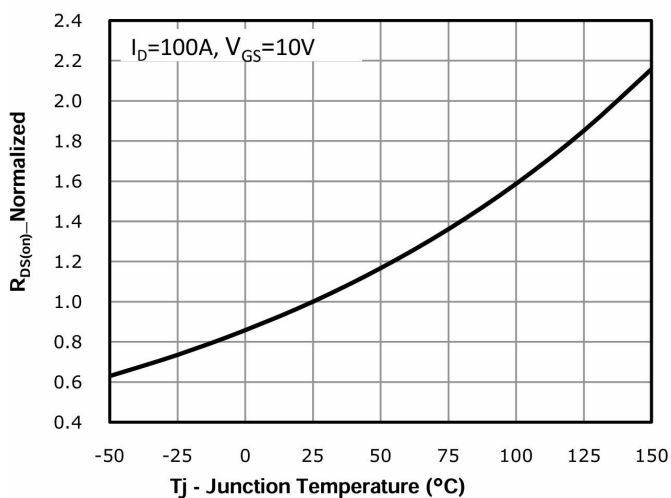


Fig 6: $V_{GS(th)}$ vs. Temperature

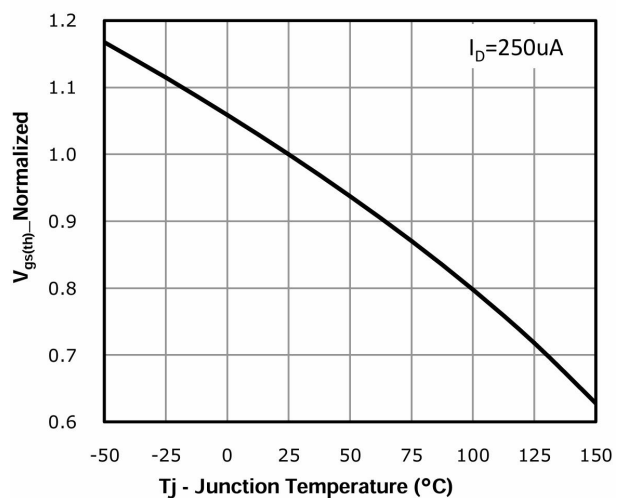


Fig 7: BVdss vs. Temperature

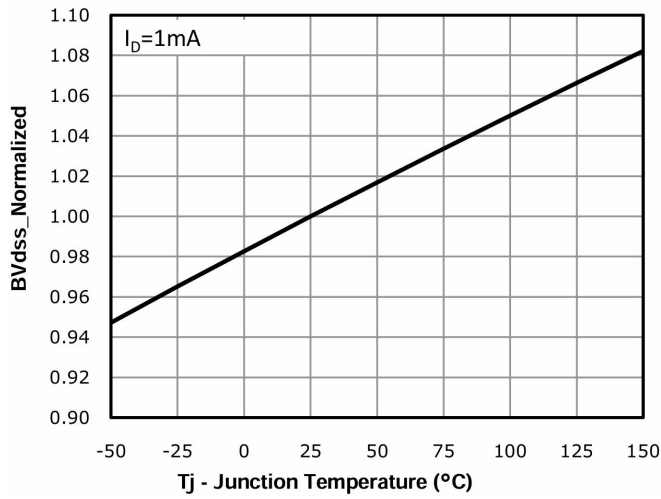


Fig 8: Capacitance Characteristics

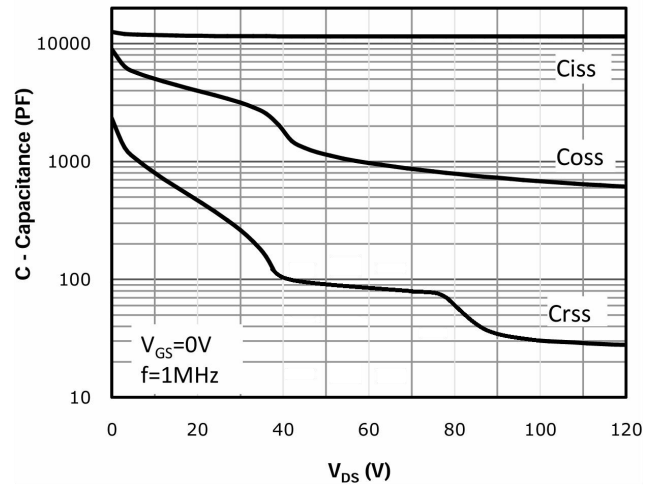


Fig 9: Gate Charge Characteristics

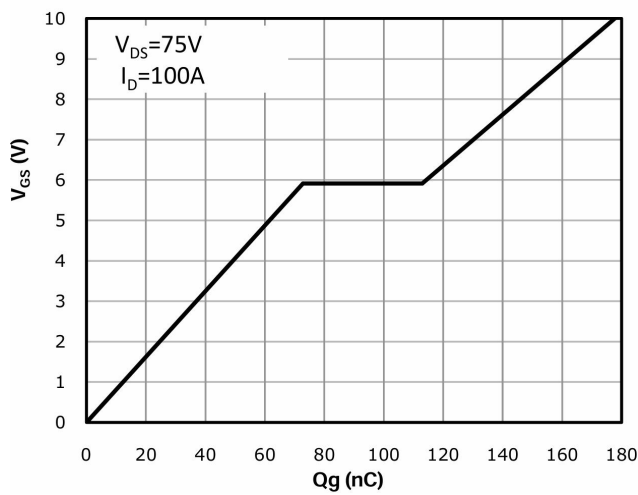


Fig 10: Body-diode Forward Characteristics

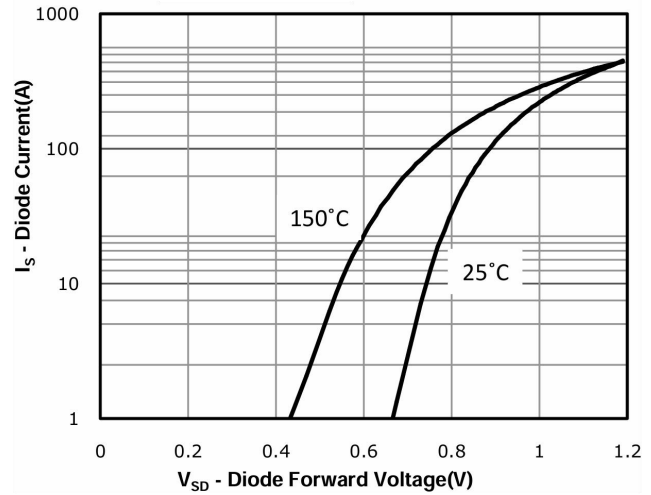


Fig 11: Power Dissipation

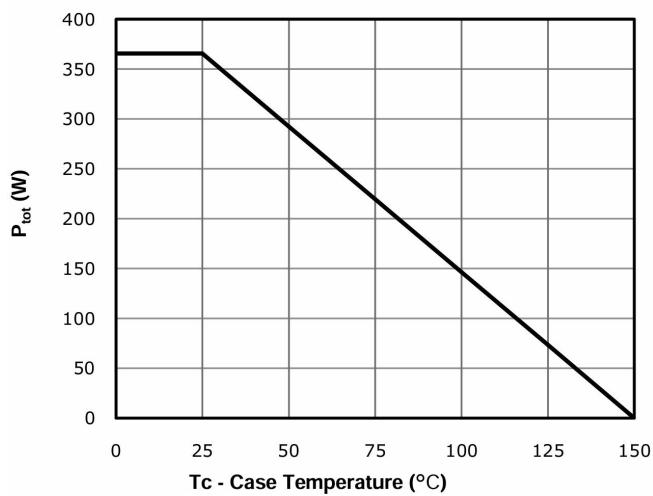


Fig 12: Drain Current Derating

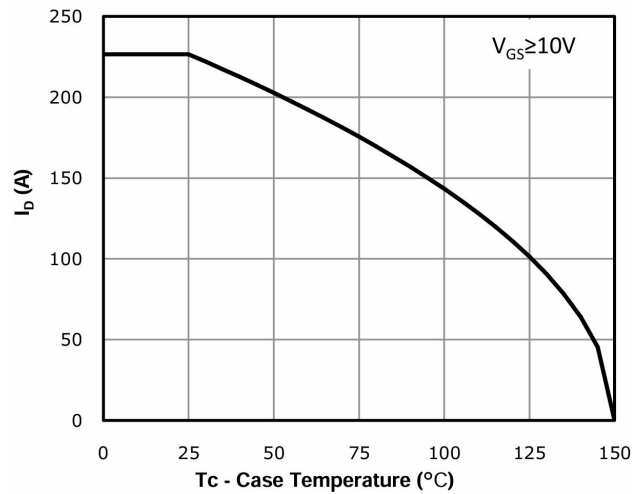


Fig 13: Safe Operating Area

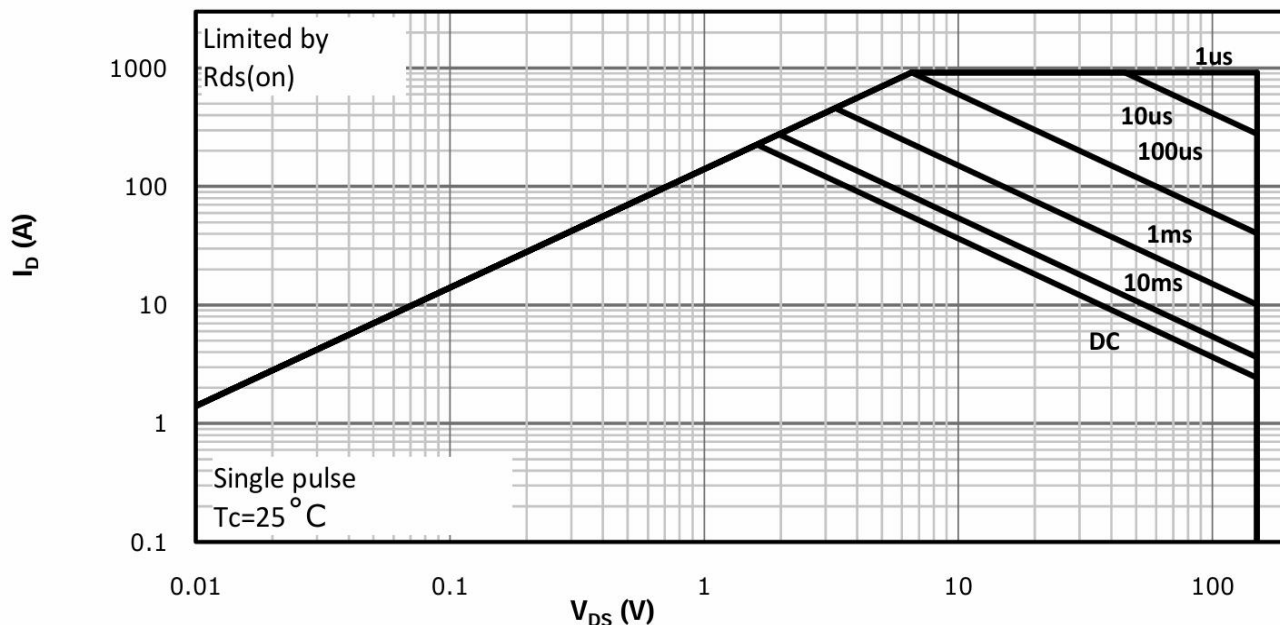
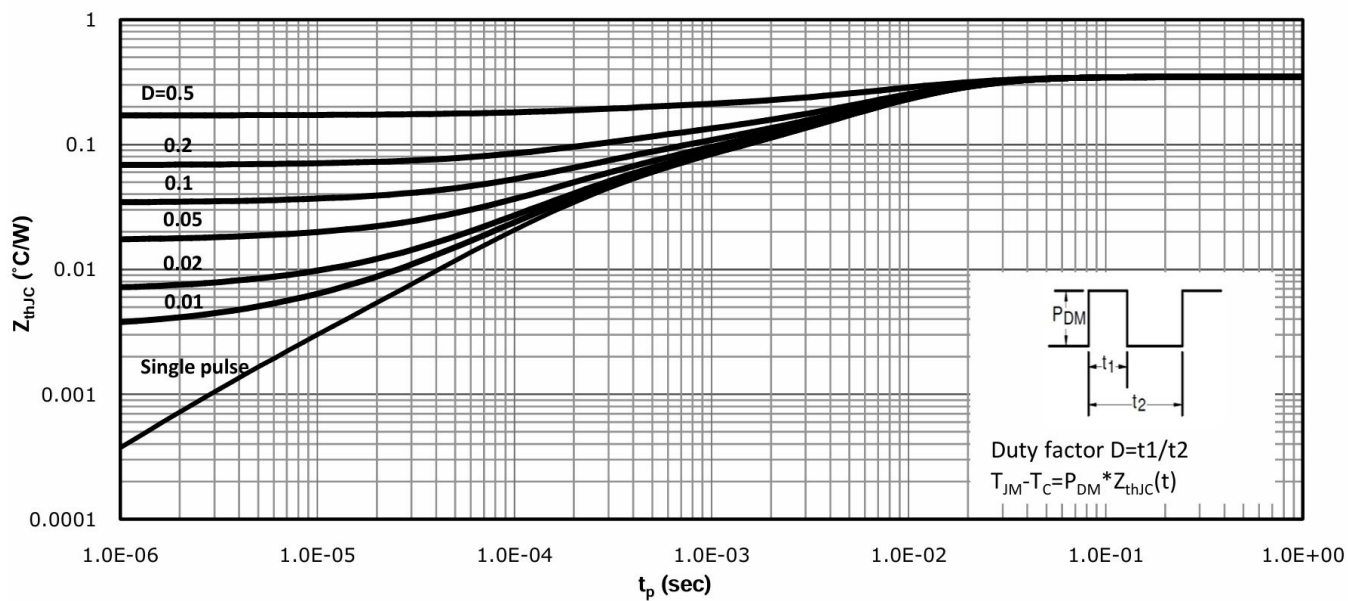
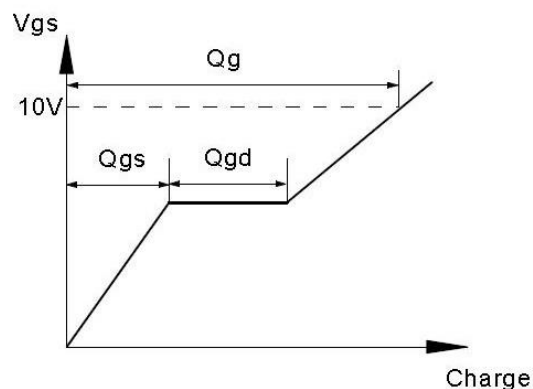
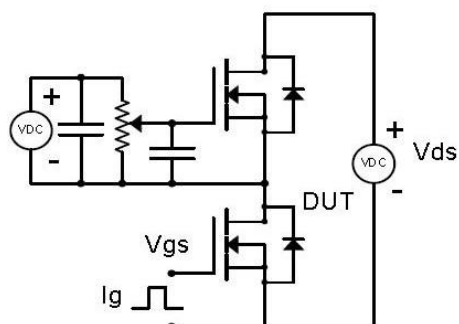


Fig 14: Max. Transient Thermal Impedance

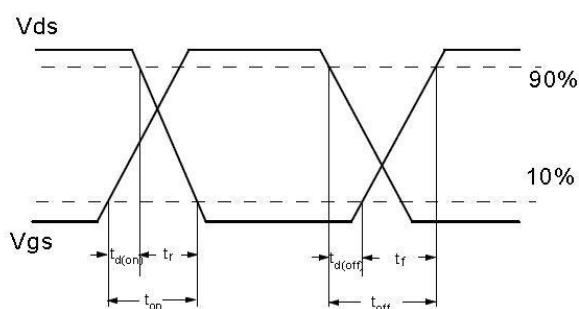
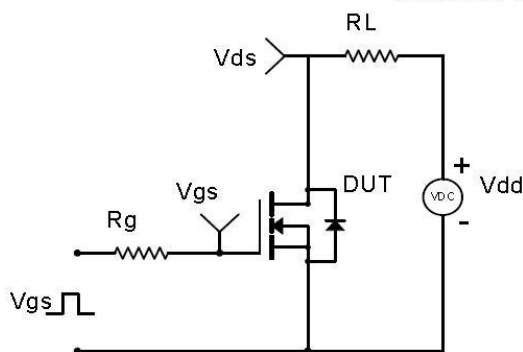


Test Circuit & Waveform

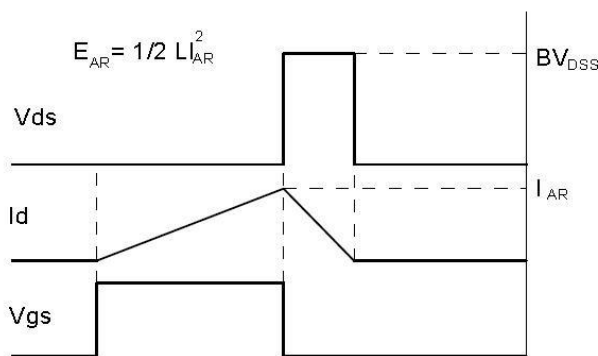
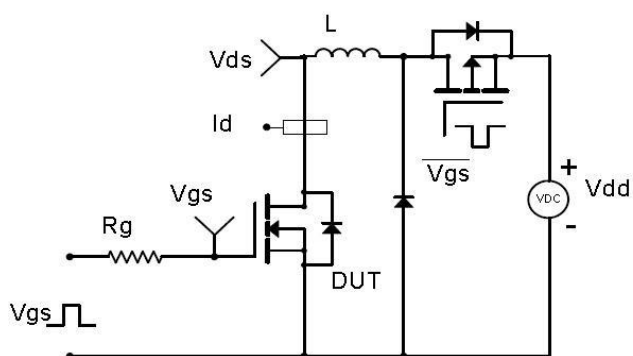
Gate Charge Test Circuit & Waveform



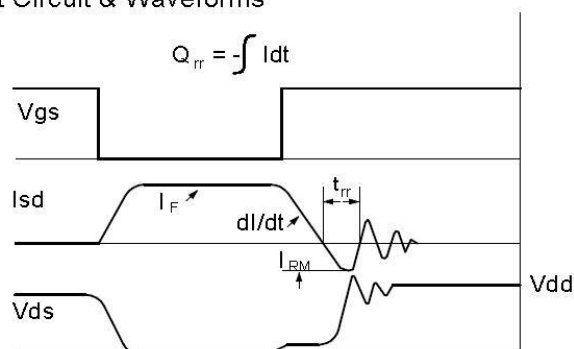
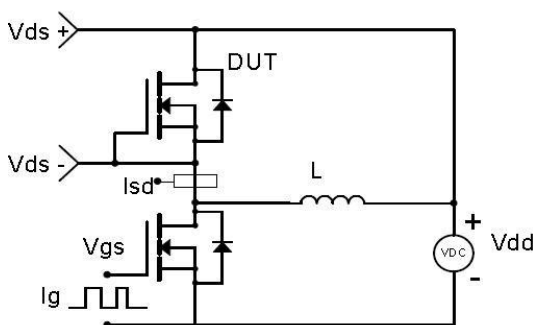
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms

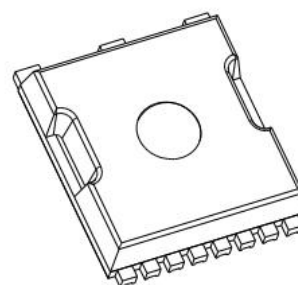
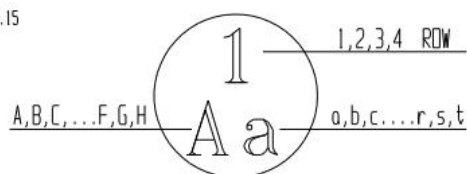
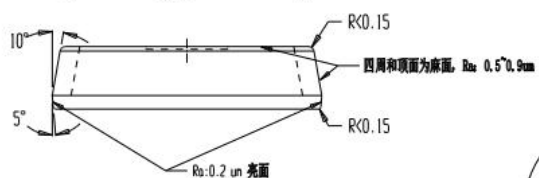
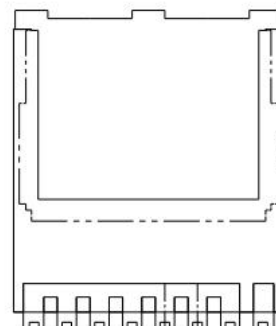
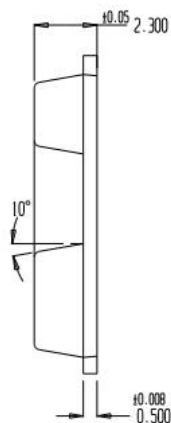


Diode Recovery Test Circuit & Waveforms



Technical drawing of a square plate with a central hole. The drawing includes the following dimensions and features:

- Overall width: 9.900 ± 0.05
- Overall height: 11.700 ± 0.10
- Inner width: 9.800 ± 0.05
- Inner height: 10.400 ± 0.05
- Central hole diameter: $\varnothing 3.000 \pm 0.03$
- Central hole position: Aa
- Distance from center to side hole center: 0.630 ± 0.05
- Side hole diameter: $\varnothing 0.30 \pm 0.05$
- Side hole position: 3.300 ± 0.05
- Bottom hole diameter: $\varnothing 0.700 \pm 0.025$
- Bottom hole position: 0.200 ± 0.025
- Bottom hole spacing: 0.750 $\times 2X$
- Bottom hole spacing: 1.200
- Bottom hole spacing: 0.200 ± 0.025
- Bottom hole spacing: (0.35)



Revision History:

Revision	Date	Major changes
1.0	2025/9/26	Release of Preliminary version.