

Features

- Uses advanced SGT technology
- Extremely low on-resistance $R_{DS(on)}$
- Excellent gate charge x $R_{DS(on)}$ product(FOM)

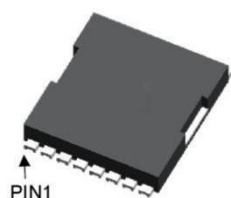
Application

- Motor control and drives
- Battery management
- DC/DC converter
- General purpose applications

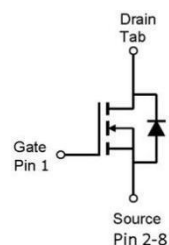
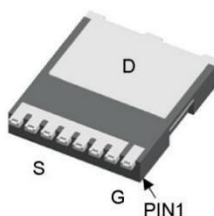
Product Summary

V_{DS}	110V
$R_{DS(on)}@V_{GS}=10V$	1.3mΩ
I_D	353A

TOLL Top View



TOLL Bottom View



Package Marking and Ordering Information

Type	Package	Marking	Reel Size	Tape Width	Qty
LR015N11ST10	TOLL	LR015N11ST10	330*28.5mm	24mm	2000

Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	110	V
Continuous drain current $T_C = 25^\circ\text{C}$ (Silicon limit) $T_C = 100^\circ\text{C}$ (Silicon limit)	I_D	353 235	A
Pulsed drain current $T_C = 25^\circ\text{C}$, t_p limited by T_{jmax}	$I_{D \text{ pulse}}$	1476	
Avalanche energy, single pulse ($L=0.5\text{mH}$, $R_g=25\Omega$)	E_{AS}	2916	mJ
Gate-Source voltage	V_{GS}	± 20	V
Power dissipation $T_C = 25^\circ\text{C}$	P_D	329	W
Operating junction and storage temperature	T_j, T_{stg}	-55~150	$^\circ\text{C}$

Thermal Resistance

	Symbol	TYP	MAX	Unit
Thermal resistance, junction – case	R_{thJC}	0.3	0.38	°C/W
Thermal resistance, junction – ambient	R_{thJA}	35	38	

Electrical Characteristic, at Tj = 25 °C, unless otherwise specified

Parameter	Symbol	Test Condition	Value			Unit
			min.	typ.	max.	

Static Characteristic

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	110	113	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$ $T_j=25^\circ C$	2	3.2	4	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=100V, V_{GS}=0$ $V T_j=25^\circ C$	-	-	1	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	±100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=40A,$ $T_j=25^\circ C$	-	1.3	1.5	mΩ
Transconductance	g_{fs}	$V_{DS}=5V, I_D=40A$	-	174	-	S

Dynamic Characteristic

Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=40V,$ $f=1MHz$	-	10208	-	pF
Output Capacitance	C_{oss}		-	4768	-	
Reverse Transfer Capacitance	C_{rss}		-	80	-	
Gate Total Charge	Q_G	$V_{GS}=10V, V_{DS}=40V,$ $I_D=40A$	-	168	-	nC
Gate-Source charge	Q_{gs}		-	61	-	
Gate-Drain charge	Q_{gd}		-	42	-	
Turn-on delay time	$t_{d(on)}$	$I_D=40A, V_{GS}=10V,$ $V_{DS}=40V, R_G=1.8\Omega$	-	38	-	ns
Rise time	t_r		-	64	-	
Turn-off delay time	$t_{d(off)}$		-	84	-	
Fall time	t_f		-	39	-	
Gate resistance	R_G	$V_{GS}=0V, V_{DS}=0V,$ $f=1MHz$	-	1.6	-	Ω

Body Diode Characteristic

Body Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_{SD}=50A$	-	0.8	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_{SD}=50A,$ $dI/dt=100A/\mu s$	-	113	-	ns
Body Diode Reverse Recovery Charge	Q_{rr}	$I_{SD}=50A,$ $dI/dt=100A/\mu s$	-	270	-	nC

Typical Performance Characteristics

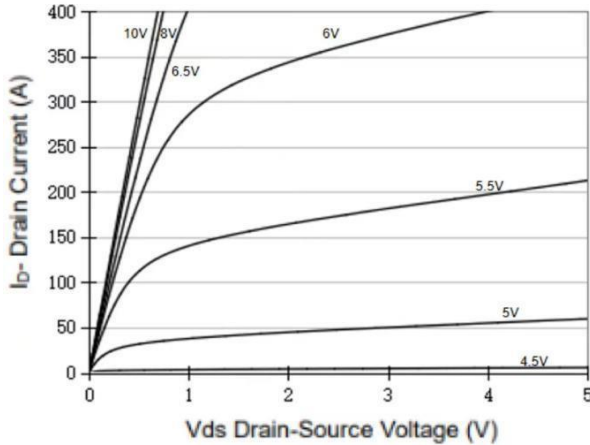


Figure 1 Output Characteristics

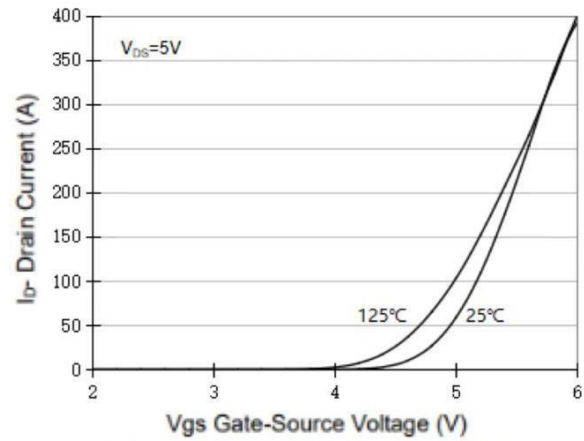


Figure 2 Transfer Characteristics

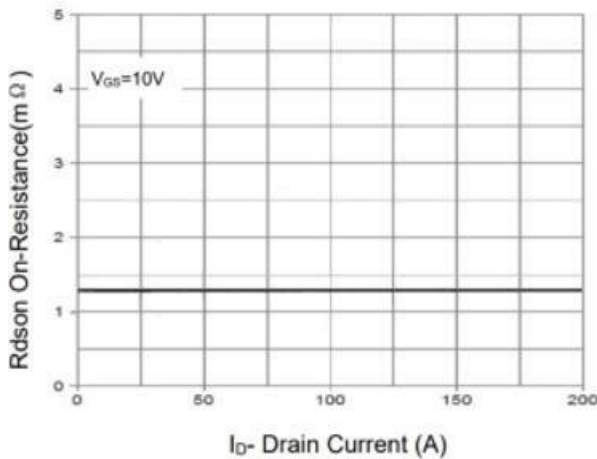


Figure 3 Rdson- Drain Current

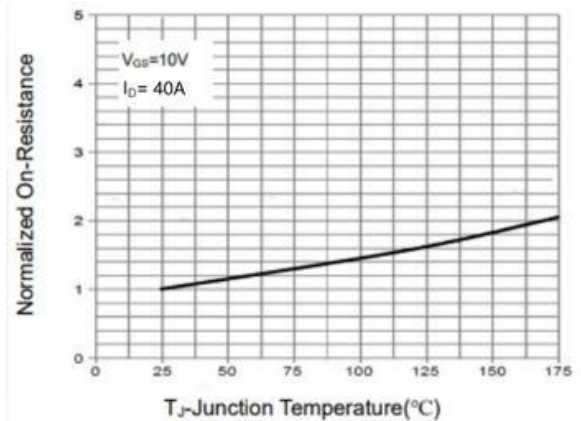


Figure 4 Rdson-Junction Temperature

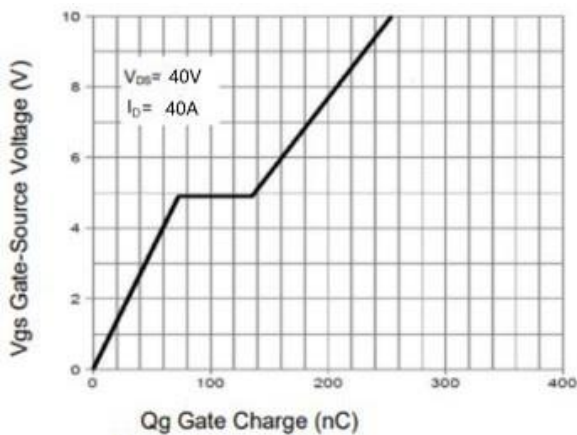


Figure 5 Gate Charge

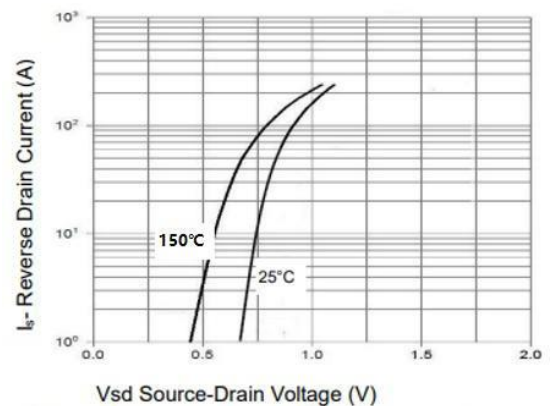


Figure 6 Source- Drain Diode Forward

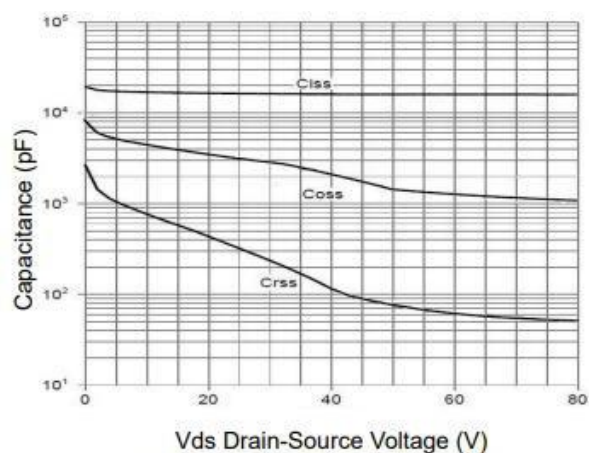


Figure 7 Capacitance vs Vds

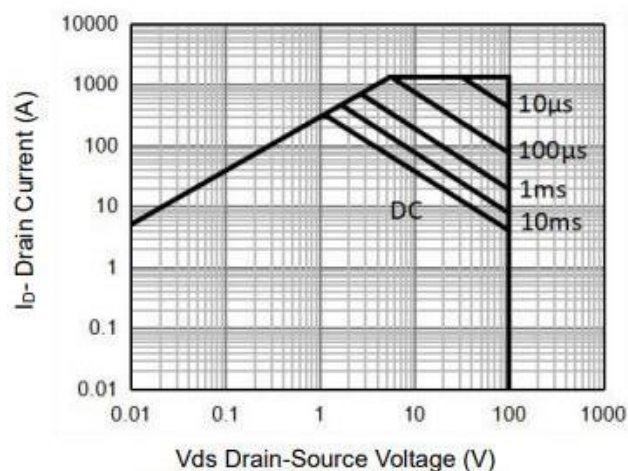


Figure 8 Safe Operation Area (Note 3)

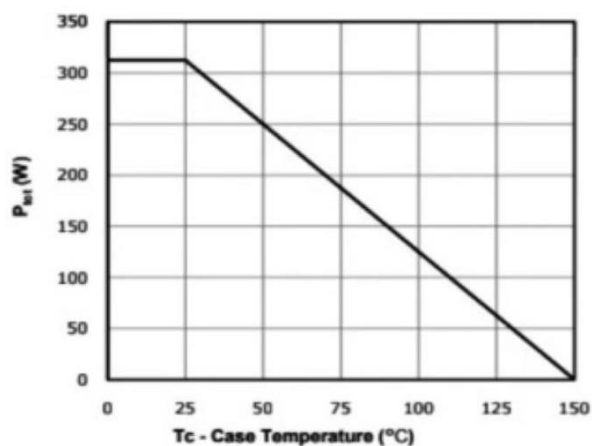


Figure 9 Power De-rating

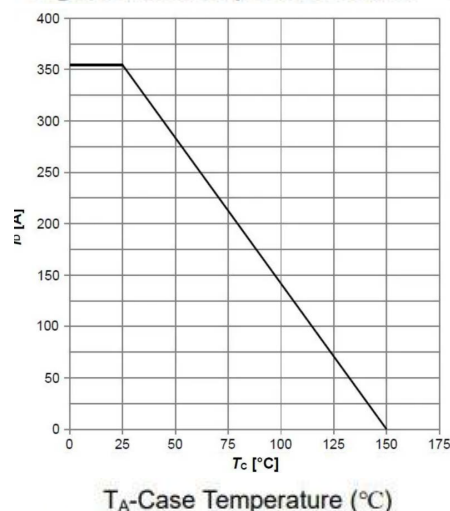


Figure 10 Current De-rating

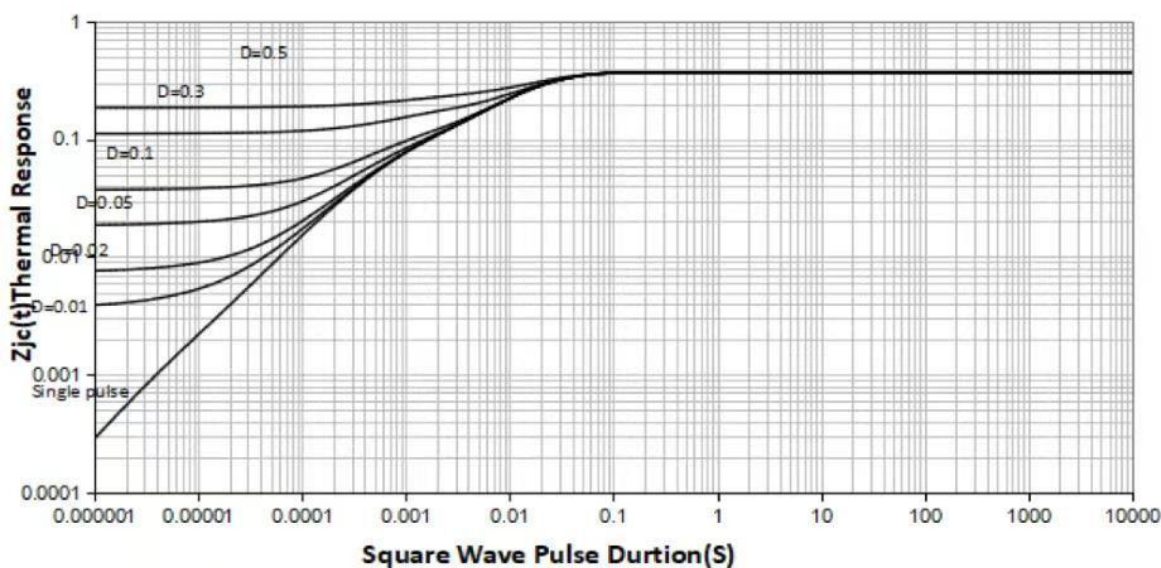
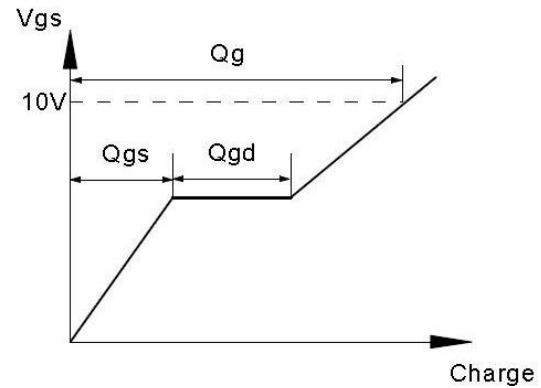
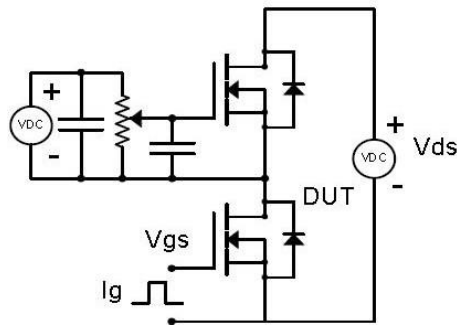


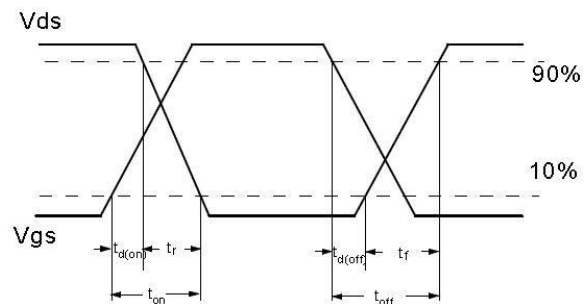
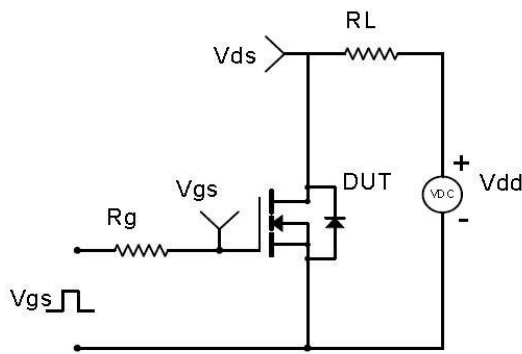
Figure 11 Normalized Maximum Transient Thermal Impedance

Test Circuit & Waveform

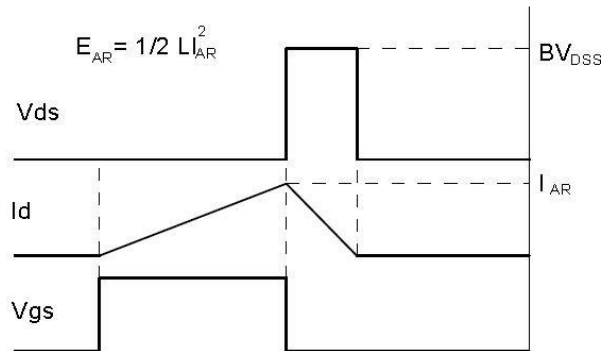
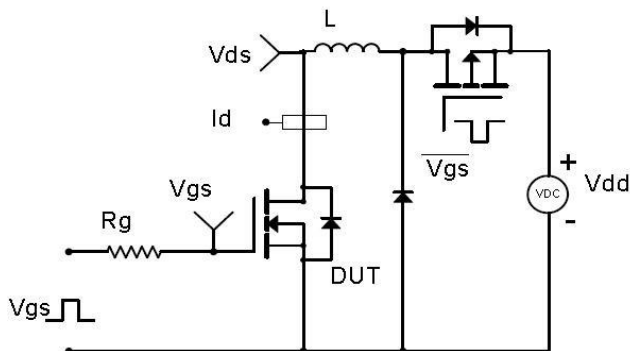
Gate Charge Test Circuit & Waveform



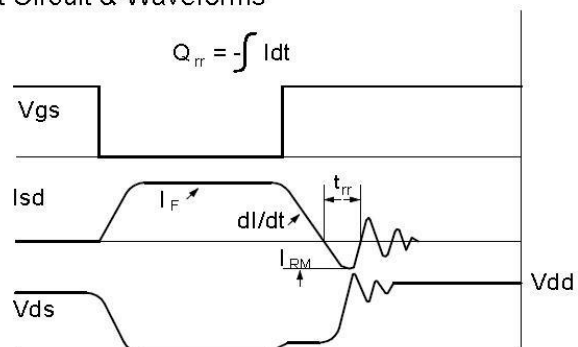
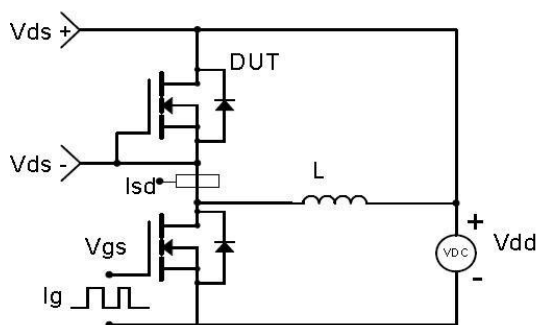
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Technical drawing of a square metal plate with a central hole and mounting tabs. The drawing includes dimensions in millimeters and tolerances. Key dimensions include: overall width 9.900 ±0.05, overall height 11.700 ±0.10, central hole diameter Ø3.0X0.10P ±0.03, and mounting tab width 0.750 ±0.025. A circular feature with '1' and 'Aa' is also shown.

